ROD-Environment Status (RODbus, ROD, GLink, Fibres)

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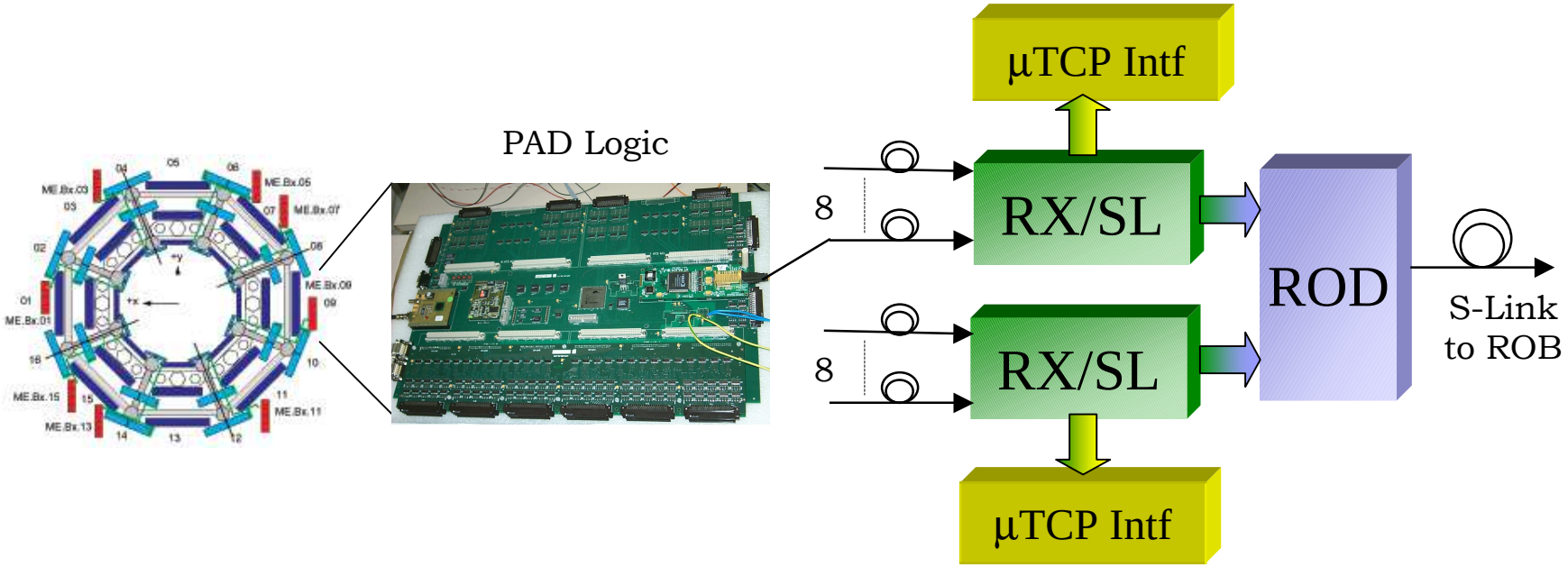
Overview

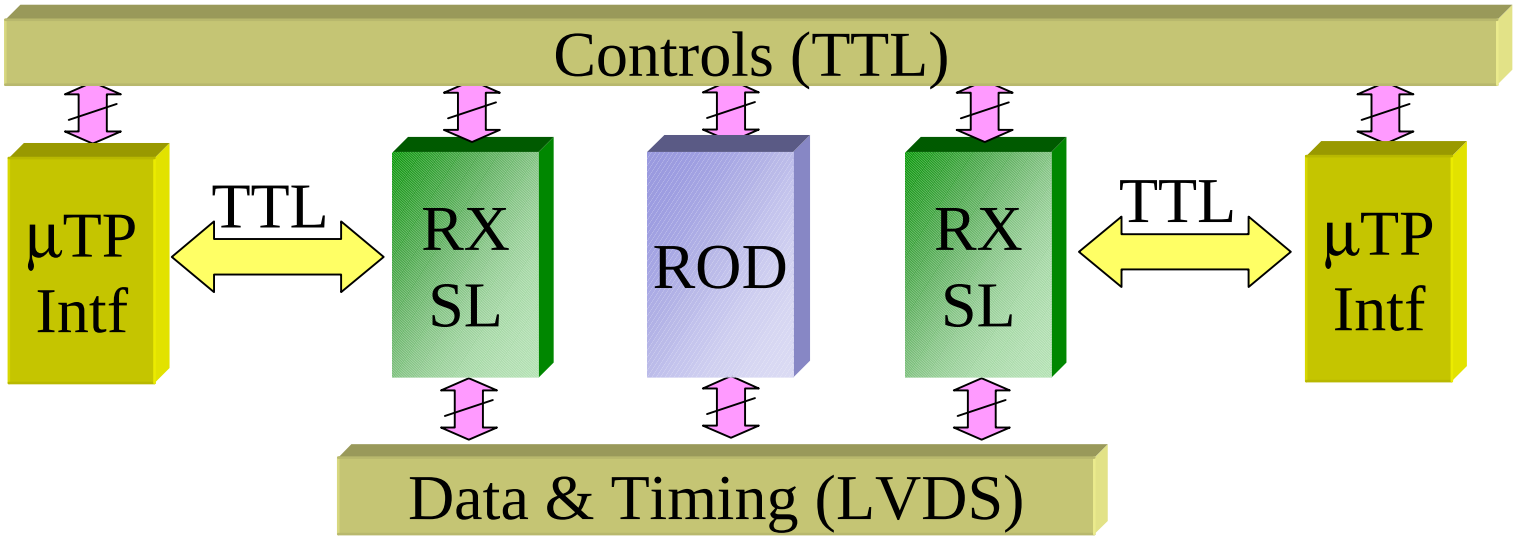
- RODbus architecture and tests
- ROD design
- Glink production status
- Fibre specifications
- Conclusions

From PAD to ROD



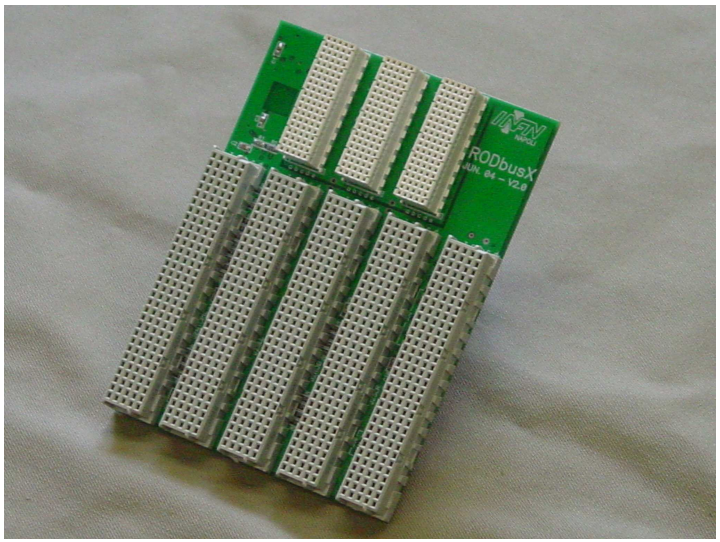
- One optical link for data and trigger:
  - 12 bit @ 40MHz on the trigger path; synch, fixed and low latency link required to guarantee timing.
  - 16 bit + strobe on the data path.

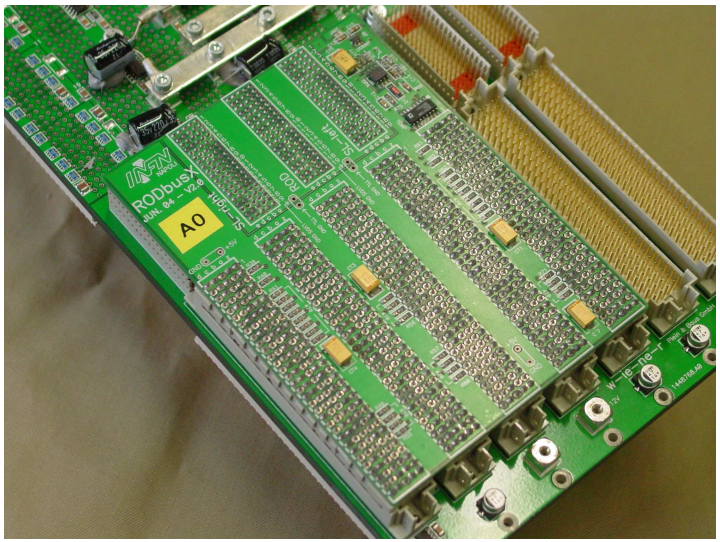
RODbus requirements



- Each RX/SL to ROD
  - 48 bit@40MHz
- Each RX/SL to µTP Intf
  - 48 bit TTL private bus
- ROD to each RX/SL
  - Timing from TTCrq
  - 8-bit TTL private bus
- ROD to all boards
  - 10-bit shared bus for controls

RODbusX-v2.0

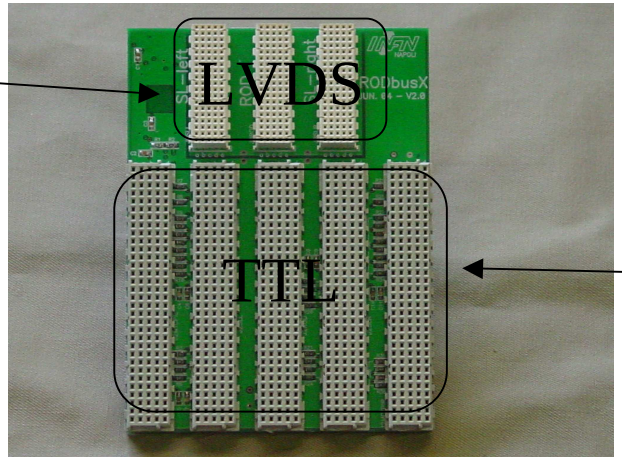




- 5-slot backplane
- 10 layer stack-up
- Diff. microstrip for LVDS pairs and single ended for TTL lines on separate planes and connectors
- Fits into the VME64x rear side

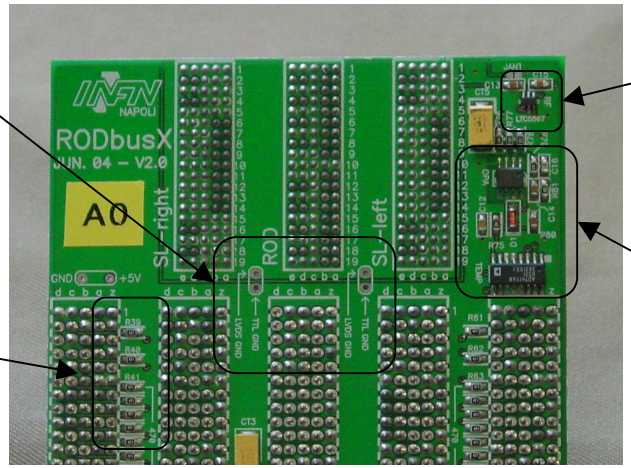
Layout

Diff. LVDS pairs routed as edge-coupled microstrips



Noisy TTL lines are routed on separate planes and connectors

Split ground plane between TTL and LVDS domains

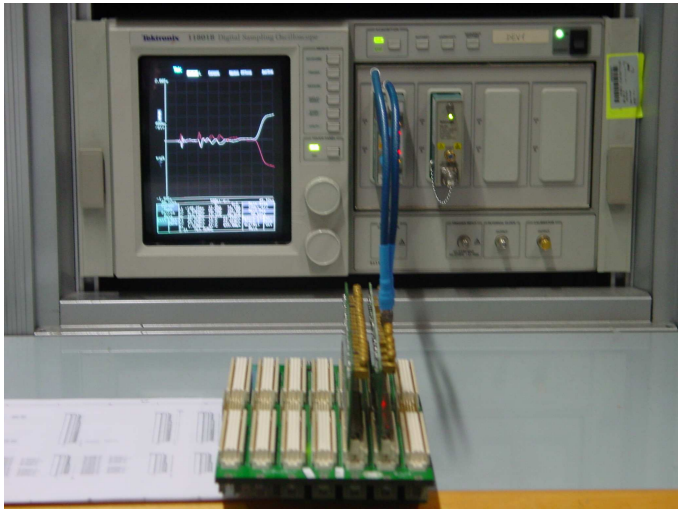


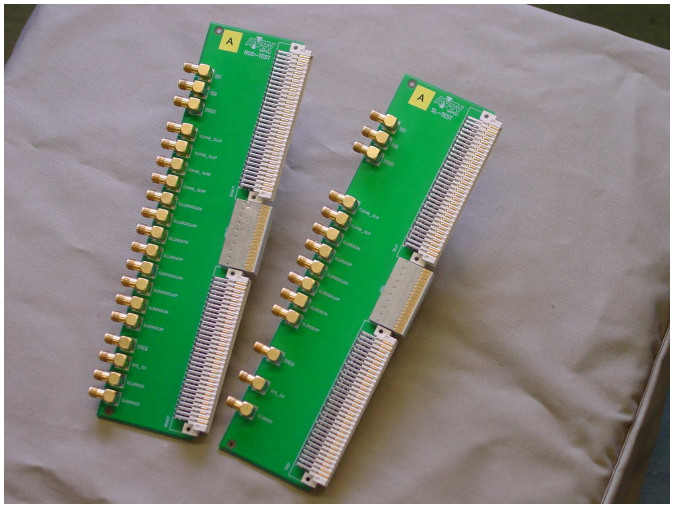
probe to monitor RF power (cellular phone like)

TTL lines terminated as VME

Temp probe and ADC to monitor power supply (both DC and ripple)

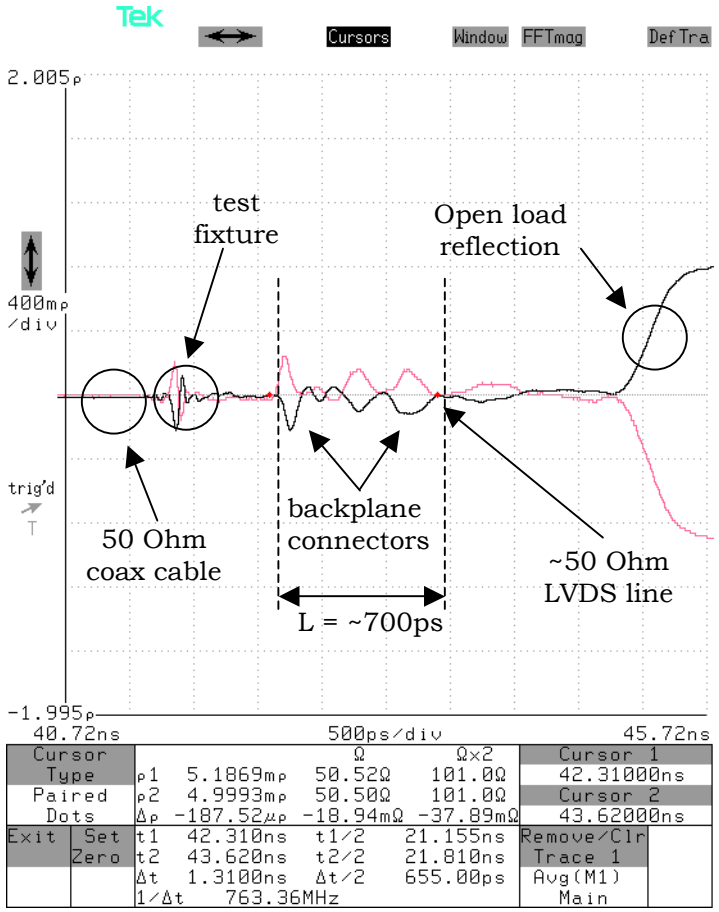
TDR test





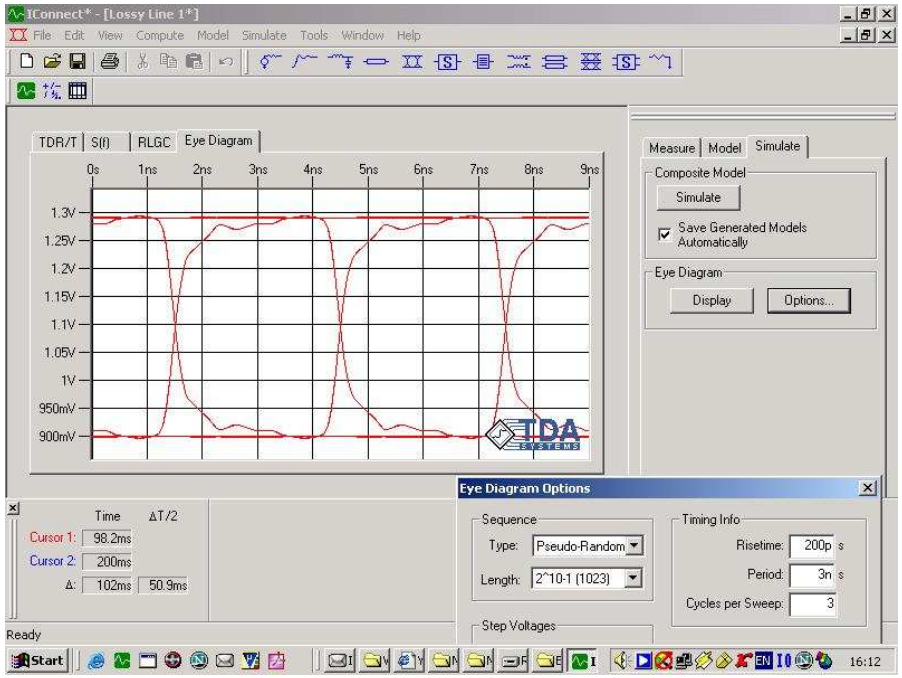
- Two test fixtures have been designed to interface the RODbus to TDR
- Diff. Impedance profile can be measured
- Impact of connectors, vias, stubs and holes (present in the real environment) can be evaluated

TDR profile



- TDR step probes backplane line and connectors
- PCB stack-up is tested
- line length and impedance are measured
- lumped L/C (connectors, vias, solder pads) are visible

System simulation



- Critical LVDS lines running @ ~330 Mbit/s have been simulated
- Simulation includes RODbus, VME64x and test features
- Eye diagrams show very good performances

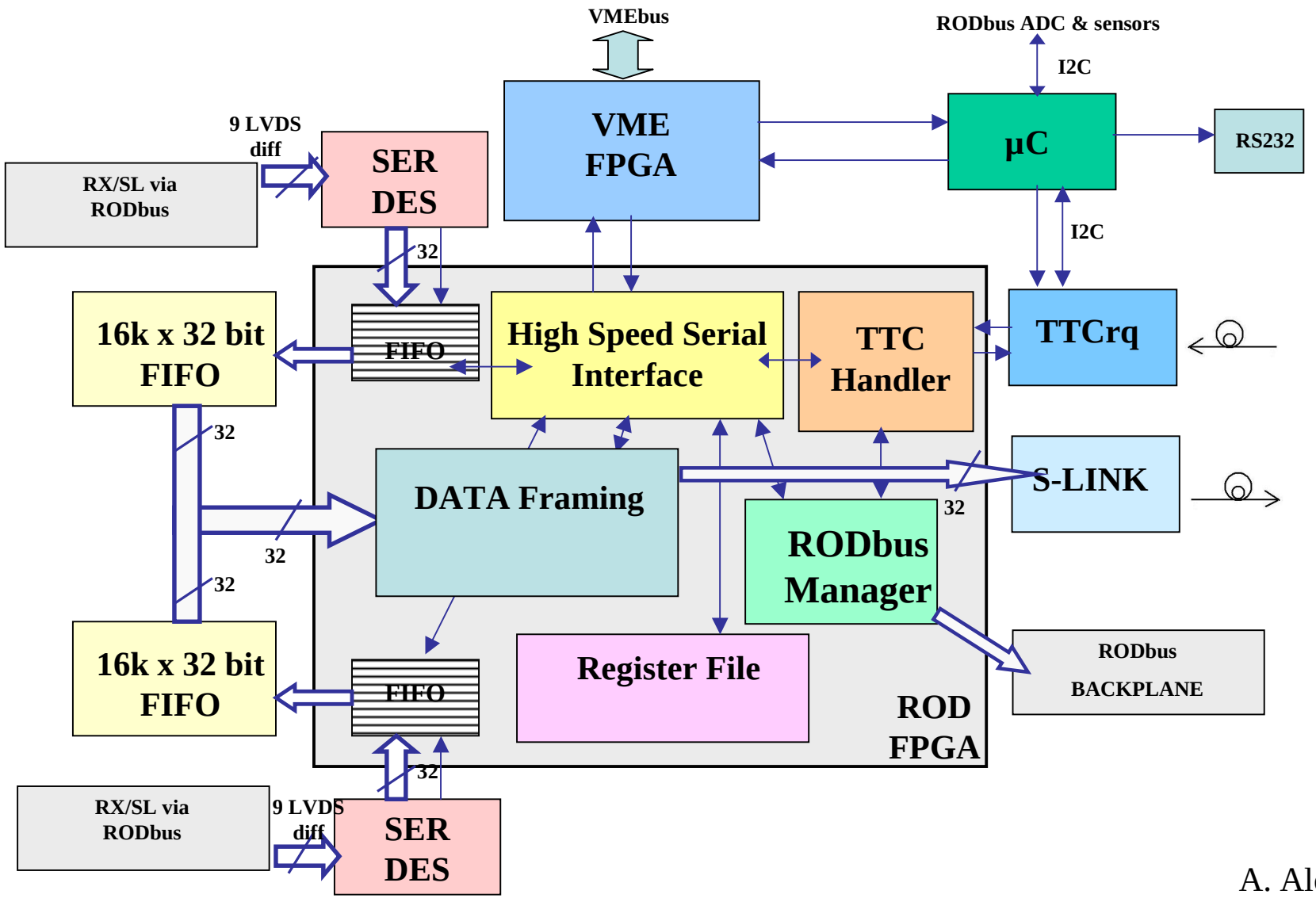
RODbus status

- Two RODbus prototypes are presently under test in Napoli and Roma
- One prototype has been used at the test-beam to link the RX-SL to the μTCP Interface
- Test results are successful, however we want to fully characterize the high-speed LVDS domain
- We expect to start the production by Apr. 2005

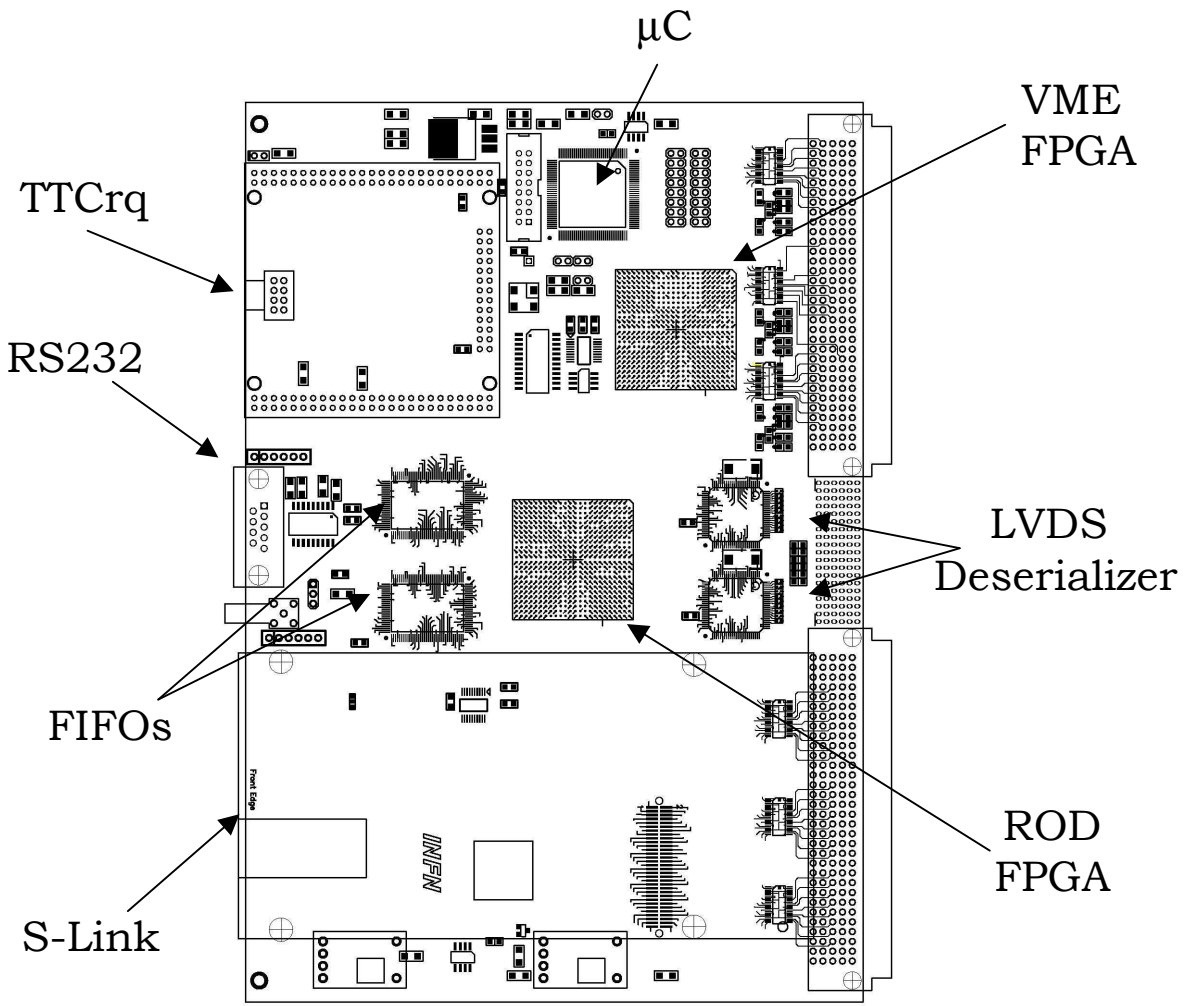
ROD board

- The design of the ROD board has started in Napoli few months ago
- At this stage, we have a flexible “open architecture” based on Virtex-II Xilinx FPGAs
- The board houses the TTCrq and S-Link mezzanines and supports all the RODbus features
- I2C operations are handled by a 16-bit μC

ROD block diagram (preliminary)



ROD layout (preliminary)



ROD schedule

- PCB ready and populated: Mar. 05

  (BGA assembly takes time and requires X-Ray validation by an external firm)
- FPGA firmware (preliminary): Jun. 05
- μC firmware: Sept. 05
- Working prototype with limited features: one year from now
- Full feature design: ??

Test bench

- Testing the ROD will require a sophisticated test bench:
  - RX/SL boards or emulators (producers)
  - ROB board or emulator (consumer)
  - RODbus
  - High level software
  - VME processor with standard DAQ platform
  - Full TTC support at home (not only the TTCrq)
- Help is needed

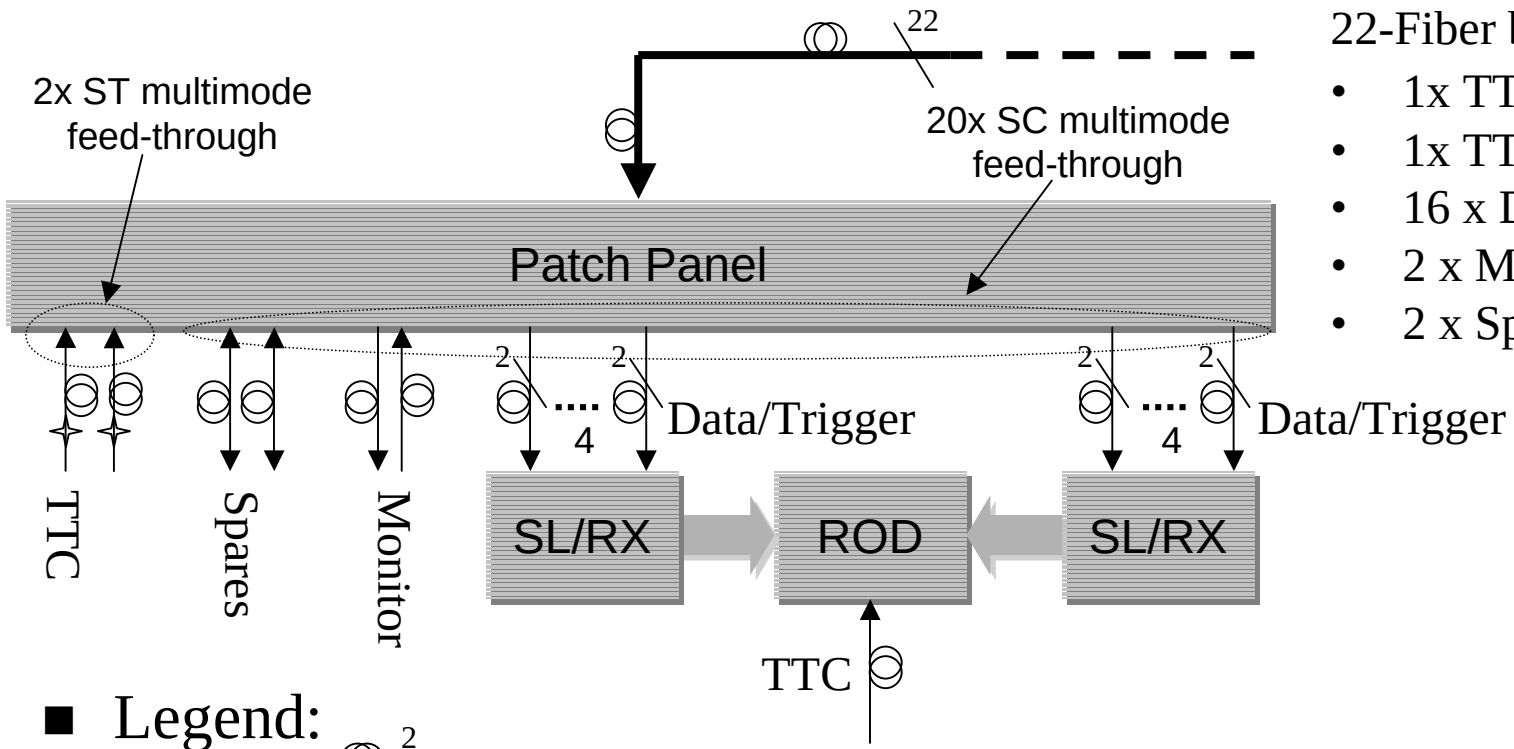
GLink

- GLink design is final and it has been successfully used the last test-beam
- ~ 20 TXs and ~10 RXs have been assembled, mounted and tested in a real environment (PAD logic, RX/SL boards)
- The production was split up into two runs: 50% in 2004 and 50% in 2005
- The 2004 run will be ready by the end of the year
- Testing the links is the MAIN issue …

Fibres

- Fiber cabling has been outlined in a short document
- Technical specs are final, however the exact layout of the “last” and “first” fiber feet depend upon the rack allocation
- We need help in order to release a final document

Fiber Layout: USA-15



22-Fiber bundle:

- 1x TTC
- 1x TTC spare
- 16 x Data/Trig
- 2 x Monitoring
- 2 x Spares

- Legend:
  - » 2 Dual-fiber patch cord (MTRJ to 2x single-SC/PC)
  - » Single-fiber patch cord (SC/PC to SC/PC)
  - » Single-fiber patch cord (ST/PC to ST/PC)
  - » 22 22-fiber bundle

Conclusions

- GLink is final and the full production is already started
- The RODbus will be ready for production in a few months (Apr. 2005)
- The ROD board is presently under development. It will take one year to get a working hardware
- We need help during the tests (links, ROD)