



## **Alma2e PCI-to-VME Bridge: Using VME 2eSST Protocol**

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### **Overview**

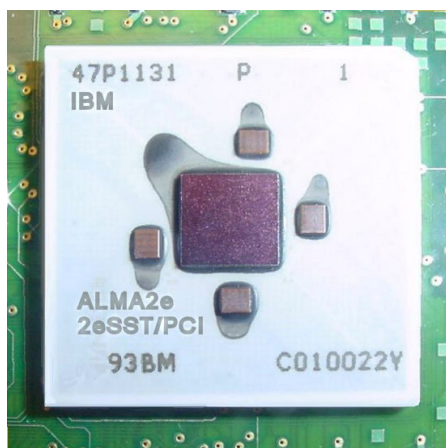
The ALMA2e is a new bus bridge designed by Thales Computers that interfaces between the PCI bus and the VMEbus. In addition to classic VME64 bridge architecture, Alma2e supports the 2e Source Synchronous Transfer (2eSST) fast transfer protocol defined in the VITA 1.5 standard. Figure 1 shows the new ALMA2e chip.

The basic VME64 features of the ALMA2e are derived from the ALMA64 VMEbus bridge that has been widely used since 1995 on Thales Computers' single board computers (SBCs). These basic features are:

- VME64 master and slave operation compliant with VME64 ANSI/VITA 1-1994
- MBLT D64, D32/D16/D08, A32/A24/A16 transfer support
- 2-channel DMA controller
- VMEbus arbiter, interrupt handler, mailbox interrupts
- Shared semaphore registers
- 1K entry PCI-to-VME mapping table for address translation and selective write post/read prefetch
- Eight VME slave windows
- 32-bit, 33 MHz PCI
- 3.3V low power design, 0.7W, 5V tolerant I/O

The new features available on the ALMA2e are:

- 2eSST transfers, up to 320 Mbytes/s
- 2eSST broadcast, allowing 2eSST writes to multiple VME slaves
- 2 Kbytes data FIFO in each direction, with programmable thresholds
- Improved MBLT64 sustained system bandwidth: 76/74 Mbytes/s for write/read with fast VME slave, 57/53 Mbytes/s for write/read between two SDRAM subsystems controlled by a PowerPC host bridge
- A64 VME addressing
- Eight new VME slave windows
- CR/CSR space
- 64-bit, 66 MHz PCI
- 2.5V low power core, 3.3V I/O, 5V tolerance on all I/O including PCI
- Low power design: 0.9W worst case with 66 MHz PCI
- -40/+105°C junction temperature
- Ceramic BGA 360 balls, 25x25 mm, 1.27 mm pitch



**Figure 1. ALMA2e Chip**

The ALMA2e has been successfully validated on two different models of Thales Computers PowerPC VME boards which are now being announced. The following sections describe the results of 2eSST operation with the ALMA2e.

### Operating in 2eSST Mode

The ALMA2e supports 2eSST transfers as defined in the VITA 1.5 standard. Only the 6U version of the standard is implemented and the slower 2eVME protocol is not supported. When the ALMA2e operates as a VME slave, up to eight addressing windows can be programmed to accept 2eSST transfers. The ALMA2e initiates 2eSST transfers over the VMEbus by using a dedicated setting of the internal DMA controller. No 2eSST transfers are generated over the VMEbus as a result of a PCI slave operation.

During **Address Phase 1** (the first DS0\* assertion), an Address Modifier (AM) encoding of 0x20 is used for 2eSST transfers. The extended AM codes used by ALMA2e as a VME master or slave are shown in Table 1:

**Table 1. Extended AM Codes**

Extended Address Modifier Codes	Address/Data Mode
0x11	A32/D64 2eSST
0x12	A64/D64 2eSST
0x21	A32/D64, Broadcast 2eSST
0x22	A64/D64, Broadcast 2eSST

**Address Phase 2** (DS0\* de-assertion) includes the cycle count and the transfer rate. For the cycle count, ALMA2e uses either the block size programmed in the DMA controller (divided by two because of the two edges) or a smaller value to avoid crossing a 2 KB boundary or to avoid transferring more data than requested at the end of the DMA.

**As a 2eSST data receiver**, the ALMA2e can accept all the transfer rates: SST160, SST267, and SST320. However, depending on particular system timing performance behavior, it is possible to not accept transfers at the SST320 rate by clearing bit 3 of the VME2ESST\_CTL register. The ALMA2e would then generate a slave error if a transfer rate of SST320 was detected during Address Phase 3.

**As a 2eSST data source**, ALMA2e generates one of three transfer rate codes (SST160, SST267, or SST320) according to its DMA\_CHN\_RATE register setting. The user programs the 2eSST timings using the register VME3ESST\_CTL per Table 2. Actual timings should correspond to a rate less than or equal to the rate code, with set-up and hold times greater than or equal to the 2eSST requirements.

**Table 2. 2eSST Data Source Timing**

Effective Transfer Rate	Speed Selection	Setup/Hold at Source ALMA2e	Number of VME_CLK (64 MHz or 60 MHz)	VME 2eSST Code (VITA 1.5 Setup/Hold at Source Connector)
146 Mbytes/s	VERY_SLOW (0x01)	23.4 ns	3.5 VME_CLK (54.6 ns @ 64 MHz)	SST 160 (18 ns)
171 Mbytes/s	SLOW (0x02)	15.6 ns	3 VME_CLK (46.8 ns @ 64 MHz)	SST 267 (10.8 ns)
205 Mbytes/s	MEDIUM (0x04)	15.6 ns	2.5 VME_CLK (39 ns @ 64 MHz)	SST 267 (10.8 ns)
256 Mbytes/s	FAST (0x08)	15.6 ns	2 VME_CLK (31.2 ns @ 64 MHz)	SST 267 (10.8 ns)
341 Mbytes/s	ULTRA_FAST (0x10)	7.8 ns	1.5 VME_CLK (23.4 ns @ 64 MHz)	SST 320+
320 Mbytes/s	ULTRA_FAST (0x10)	8.35 ns	1.5 VME_CLK (25 ns @ 60 MHz)	SST 320 (9 ns)

During **Address Phase 3** (DS0\* reassertion), if a broadcast 2eSST operation has been selected (XAM 0x21 or 0x22), VME addresses A21 to A1 indicate the geographical address of the slaves to be targeted by the broadcast. To select a slave with a geographical address *i*, bit *Ai* should be set to 1. For each DMA channel, the slaves participating in the broadcast operation are programmed in register DMA\_VME\_SLVSEL.

**During the broadcast operation**, the master responds with DTACK\* to its own cycles, and the participating slaves capture the transmitted data. If a slave is not ready to accept the full broadcast operation, it asserts RETRY\* during Address Phase 3 to request the transfer to be restarted.

## Measurements and Validation in 2eSST Mode

ALMA2e and 2eSST operations have been successfully qualified on two Thales Computers VME PowerPC boards:

- a VME SBC based on the IBM 405GP PowerPC, including 64-bit PCI at 66 MHz that interfaces to Alma2e.
- The brand new V4G4c, a 6U single slot VME quad-processor computing node featuring four 500 MHz Motorola MPC7410 PowerPC processors, a system bus at 133 MHz, up to 1 GB of on-board SDRAM, 2 independent PCI buses (64 bit/66 MHz and 32 bit/33 MHz), 2 PMC free slots, up to 32 MB of Flash EEPROM, one Ethernet T100, 4 serial lines, PCI64 expansion to P0 to accommodate up to 4 PMC cards in two VME slots, and the VME 2eSST interface to the backplane.

The 2eSST operations have been exercised alone first, and then under operating system activities, with multiple simultaneous transfers, and with both 2eSST and standard VME cycles. During all the transfers, data integrity checks were successful at all rates and performance matched the expected theoretical transfer rates.

Figures 2 and 3 show a global snapshot of the beginning of a 2eSST transfer at the ALMA2e receive pins for read and write.

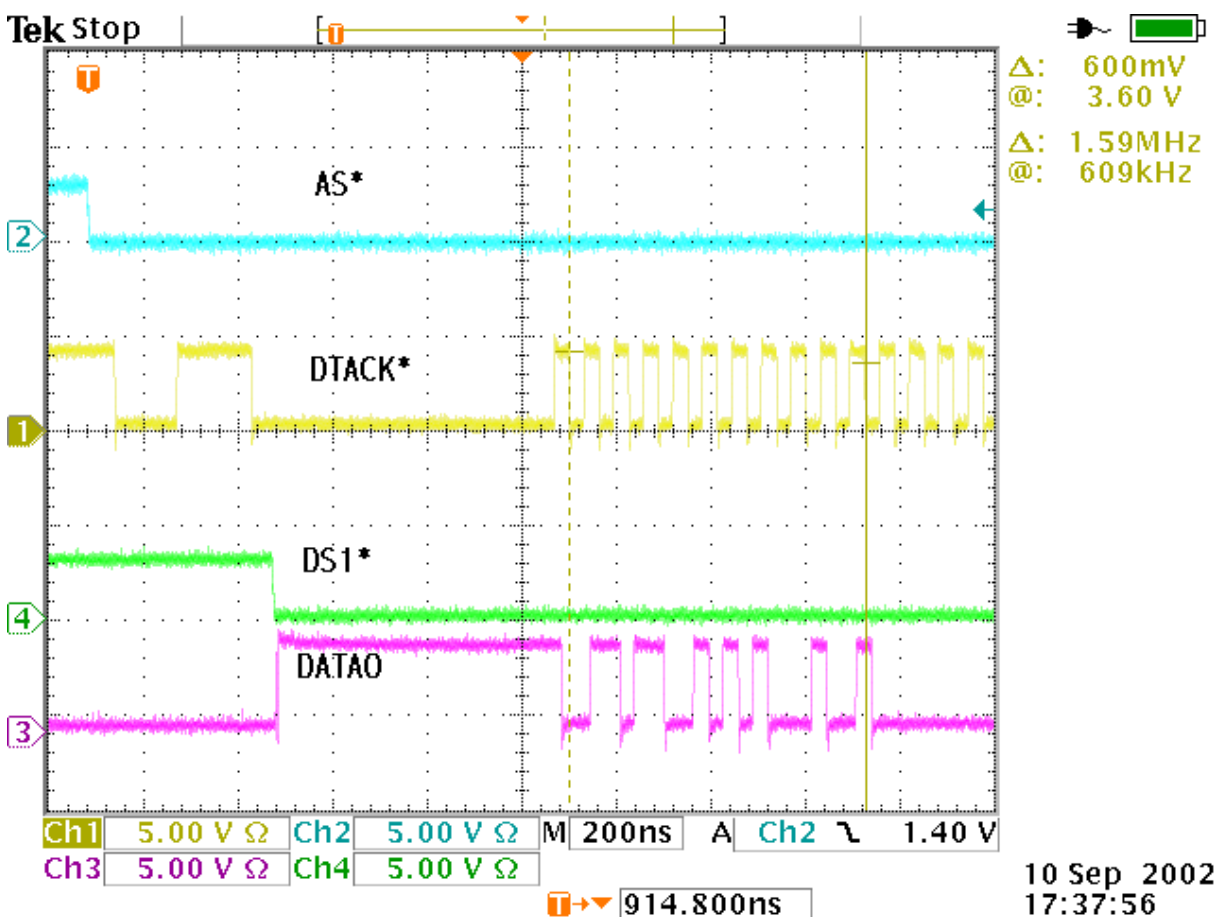
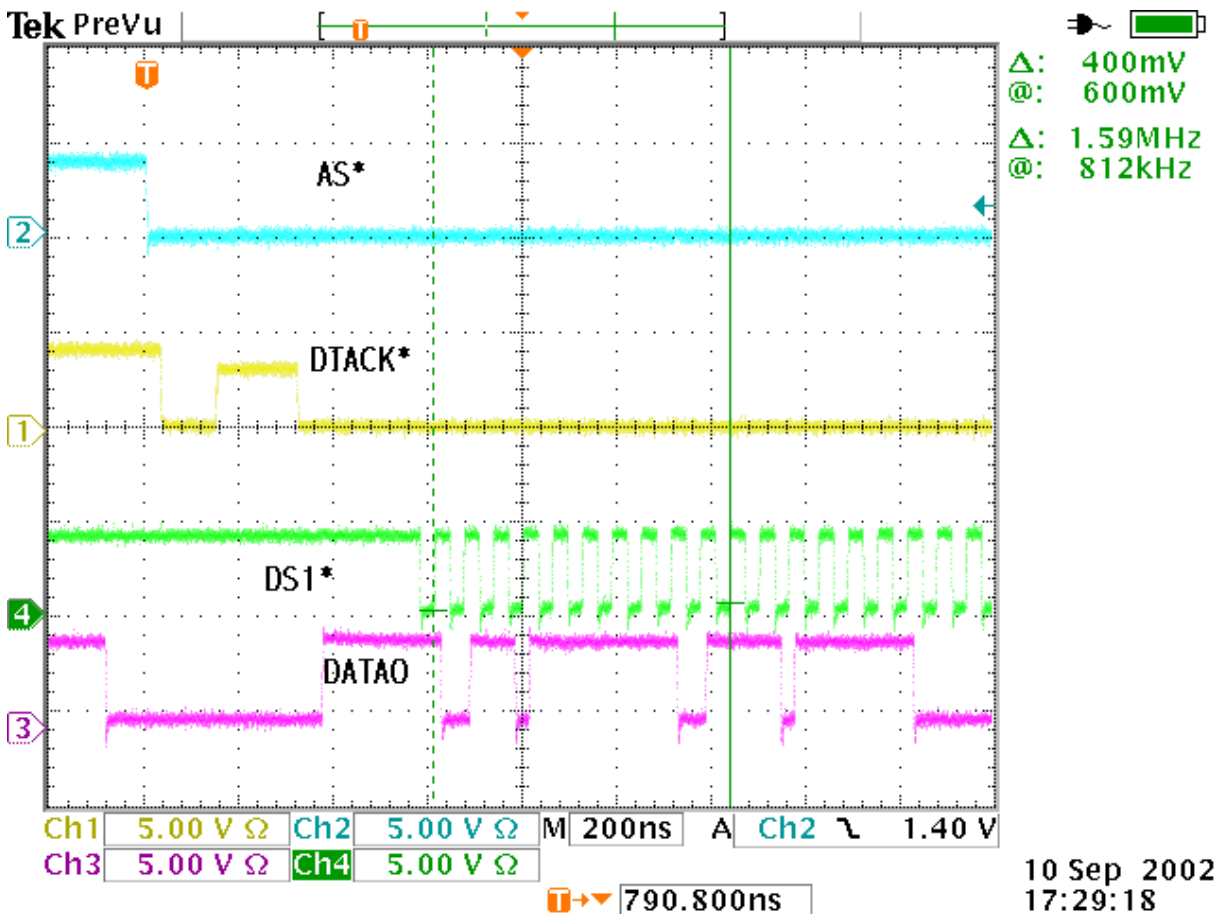


Figure 2. ALMA2e 2eSST Read Timing

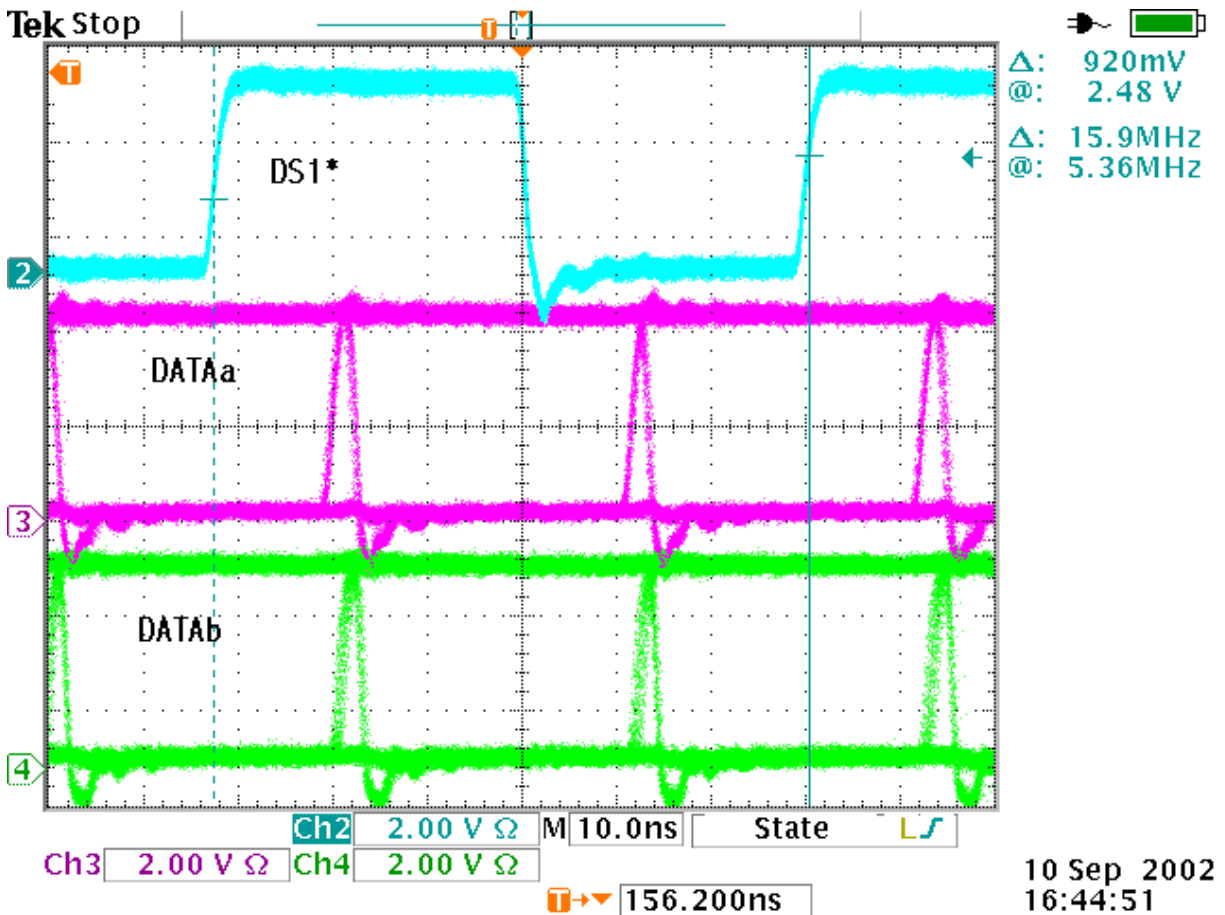


**Figure 3. ALMA2e 2eSST Write Timing**

The transfer rate achieved during the burst phase of the 2eSST transfers in Figures 2 and 3 can be calculated as follows: the distance between the two cursors represents a rate of 1.59 MHz; during this time there are 10 clock periods corresponding to the transfer of 8 bytes on the positive edge and 8 bytes on the negative edge. Thus, the transfer rate during the burst is  $16 \times 15.9 = 254$  Mbytes/s.

For a 2-Kbyte, 2eSST write transfer, if we take into account the initial 600 ns period spent during the three address phases, the effective rate is in fact close to 240 Mbytes/s. For read timing, the initial phases before transferring the data last longer (about 1  $\mu$ s in the scope capture) because ALMA2e has to read the data first from the PCI.

The timings provided on Figures 2 and 3 were captured with ALMA2e programmed at SST267 and speed selection FAST. With the same settings, Figure 4 represents the typical setup and hold time as seen by the ALMA2e receiving the data. A 2eSST write is shown, but the read diagram looks the same with DTACK\* transitioning instead of DS1.



**Figure 4. Setup and Hold Time During a 2eSST Write to the ALMA2e**

### Thales Computers' Boards Support 2eSST Now

The brand new V4G4c (Quad-processor computing node based on MPC7410), just announced by Thales Computers, features the 2eSST protocol on the VME thanks to Alma2e. The board is available now.

The V4G4c is VITA 1.5 compliant. It implements the traditional 5V VME buffers. For this reason, the use of the 2eSST transfers has been restricted to standard backplanes that do not exceed six slots in order to prevent signal reflection on 2eSST clocks. For configurations requiring a backplane with more than six slots, system integrators using 2eSST transfers must ensure that the proper VME64 or VME64x backplanes and boards loaded into the system will allow for monotonic rising and falling bus signals through the threshold region of the receiver (VITA 1.5 rule 3.2).

Thales Computers will be introducing a processor board featuring the new enhanced VME transceivers, SN74VMEH22501 from Texas Instruments, to take advantage of the 2eSST technology over a full 21-slot standard VME64x backplane.

ALMA2e is supported at the operating system level through drivers available under VxWorks, LynxOs and Linux.

At the system level, the high bandwidth of 2eSST transfers and the broadcast capability enables building efficient computing and I/O architectures, often saving the cost of specialized I/O channels for small configurations.

## Summary

The new ALMA2e PCI-to-VME bridge designed by Thales Computers offers several functional enhancements over the previous generation of VME bridges. The implementation of the 2eSST transfers allows the design of a glueless VITA 1.5 VME interface operating at up to 320 Mbytes/s on a standard VME64x backplane.

Signal and data integrity during 2eSST operation have been successfully qualified on two Thales Computers models of VME computer boards: a test board featuring the PowerPC 405GP chip and the new V4G4c computing node implementing four MPC7410 PowerPC chips.

The VME computer boards are available now and are ready to use 2eSST transfers. The support of multiple operating systems like VxWorks, LynxOs and Linux gives the integrator greater flexibility in defining the system architecture. The support of the 2eSST broadcast capability may also bring a decisive advantage in some I/O-intensive configurations.

## THALES COMPUTERS

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