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The VIRGO Data Acquisition System

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Abstract

The experimental environment of the VIRGO project which is in construction will be briefly described. A number of issues for data handling in the online environment including real time aspects will be outlined. The Data Acquisition System which has been designed will be presented.

We shall describe the overall architecture of the VIRGO Data Acquisition System and the baseline design of components which fulfill experimental requirements. Particular emphasis will be given to the distributed readout system which operates at a sampling frequency of 20 kHz and the data collection scheme which operates over large distances.

I. INTRODUCTION

The Virgo project of direct detection of gravitational waves is carried out by the INFN (Italy) and CNRS (France) [1]. The Virgo antenna shown on Figure 1 is basically a Michelson interferometer, with perpendicular arms of 3 km each and Fabry-Perot resonant cavities which increase the equivalent optical length for each arm. An external recycling mirror is added in order to increase the light power in the cavities, while optical components are seismically insulated by means of special suspensions including multi-pendular chains.

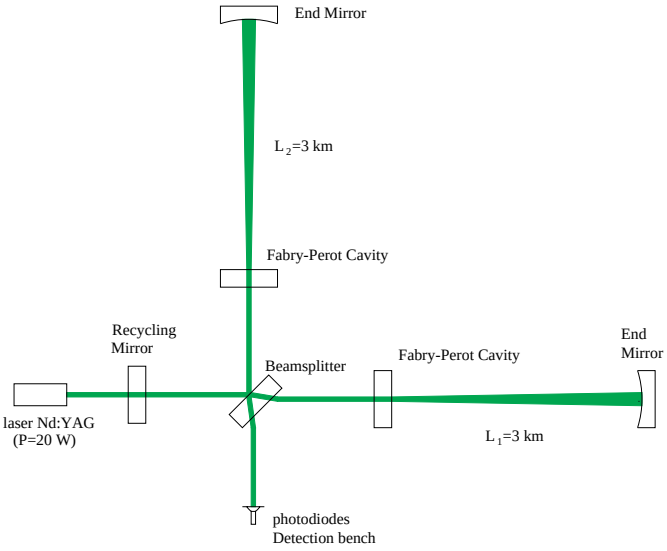

Figure 1: Virgo antenna conceptual scheme

The interferometer will be operated under vacuum. A very stable Nd :YAG laser is used as the light source. Two beams are produced by a beamsplitter and then recombined out of phase. The interferometer is then locked on a dark fringe. Any variation of the optical path's length, caused by the passage of a gravitational wave, produces a partial phase shift of light beams in the two arms and will be detected by photodiodes.

The experimental setup of VIRGO will be sensitive to a wide spectrum of frequencies, from 10 Hz to a few kHz in order to get the best chance of detecting radiations from fast and massive sources in our galaxy or nearby ones, such as fast rotating neutrons stars, supernovae, and coalescent binaries.

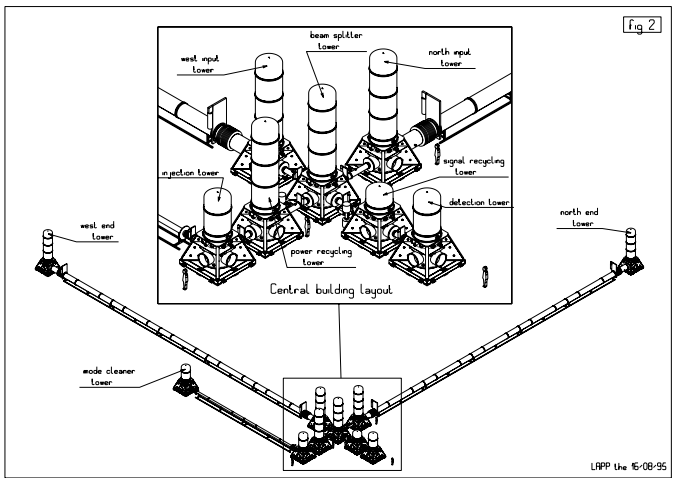

Figure 2 : Virgo layout with details of the central vacuum system

The needed infrastructure, shown on Figure 2, consits of a pair of 3 km long tunnels, a large vacuum system, vacuum towers for containing the suspensions of the optical components including experimental halls, central and terminal buildings. The construction of Virgo started in 1994 in Cascina near Pisa (Italy) and the first data will be taken in 2001.

II. THE ONLINE SYSTEM

Such an instrument requires an automatic control system in order to bring the various components close to the interferometer working point and then to keep them in a range that maintains the required sensitivity of the overall instrument. This is done by a high-speed low-noise digital control system.

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Most of the signals produced by the different sensors are processed by a layer of local controls which apply local corrections to keep the controlled elements (laser, mirrors, vaccum pumps..) within a given set of tolerances. These controls produce status information and feedback values which are collected by the Data Acquisition System together with the digitized information produced by the various active parts of the detector: the laser system, the interferometer and the detection bench.

A. Online Architecture

The online architecture preserves flexibility in the interferometer setting up and takes account of the large distances which may separate two components. The control systems are organized as much as possible into independent units in charge of the adjustment of a well defined component. Similarly, the readout systems are implemented into independent units in charge of the collection and the concentration of the data produced near the components located in the same building: end mirror west and north, mode cleaner and main buildings. A central data acquisition system, located in the control room, collects and assembles these raw data. Then several tasks are performed in parallel. First the raw data archiving system [2] archives all frames on DLT tapes, making it possible any retrieval and reprocessing of original data. The online preselection reduces the amount of raw data to a level manageable by the offline analysis. It computes physical quantities from the raw data, runs online analysis algorithms and selects the frames in which a gravitational wave candidate may occur. Finally, the 'selected' data and subsets of the non-selected ones are sent to the data recording and distribution system which is the experiment front end for the offline analysis. The data quality is also permanently monitored by surveying the noise level and a known signal which is produced by a calibration device and which stimulates the interferometer as a gravitational wave would do.

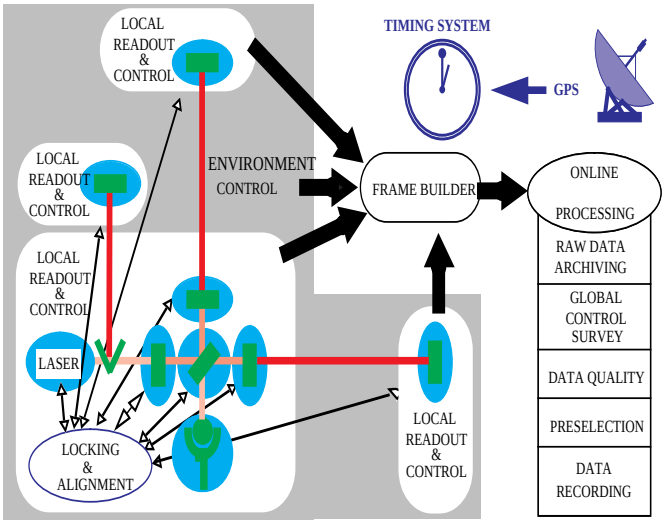

Figure 3: Virgo online architecture

The knowledge of the precise timing of the various measurements and actions performed around the interferometer is one of the key points of its operation as a gravitational wave detector. This is implemented with a central timing system, located in the control room which is set up to distribute a well defined clocking sequence all over the site.

Figure 3 shows the overall online system. The environment control delivers status information sampled at a low rate. The locking and alignment system of the interferometer includes various servo loops and delivers both detector and auxillary information (such as feedback values) sampled at much higher rate.

B. Hardware Options

Sensors, processors, and their actuators sampled at high rates are implemented within the commercially available VME standard. In order to execute the various feedback loops within a constant time, the VIRGO online system has to be built with conflict free accesses. Thus, high transfer rate digital servo loops are implemented with a dedicated bus and conflictual bus accesses are avoided by housing only exclusive controls in the same crate. Higher level control and acquisition processes transfer their information from one building to an other, using point to point communications over Digital Optical Links (DOL). Short distance transfers may be performed using local vertical bus as well.

The environment status is generally measured with sensors sampled at a low rate implemented in VME or G64 which are read out by slow monitoring systems. These data are exchanged using a dedicated ETHERNET network (the slow monitoring network) extending over the site.

All the processors are networked via ETHERNET or FDDI and are accessible for control and file exchange by all workstations. The networking between the main building, end mirror buildings and the control room has been designed in such a way that hardware links are used for any real time connections while computer networks are used for state control and for slow monitoring.

C. Software Options

The various online processes are designed as standalone tasks getting data from a dedicated local sensor and/or from another process and organized to operate under the mastership of a supervisor. As shown on figure 4, each real time process which has direct access to the hardware (typically ADC's, servoloop,...) is usually running on a VME CPU board and conceived as a server in the framework of the client-server model. User interfaces are client processes running on workstations and are used to configure server processes, monitor or display data. Several user interfaces can be simultaneously used over the same server to monitor its information, but only one client at a time (the master client) has the privilege to configure it. Possible conflicts are locally solved using standard rules and information provided by the

online database. The error logger is the last server which should always be running. It collects the information and error messages from all the processes. The error display is the error logger client which provides the tools to select and display error messages collected by the error logger.

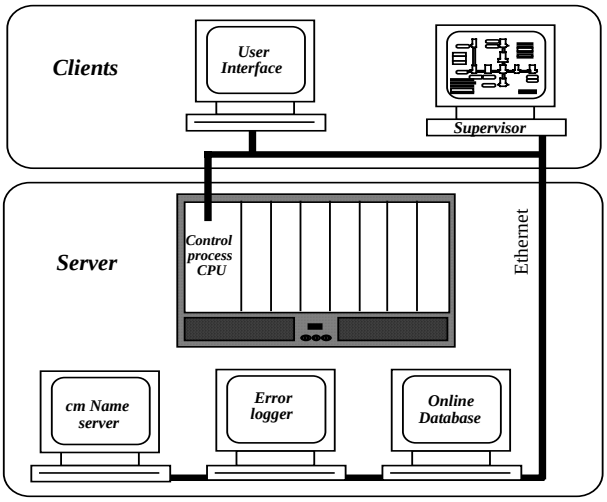

Figure 4: The online client/server organization

The VIRGO collaboration has chosen C language as the programming language and LynxOS as the real time operating system.

III. Data Acquisition System

A. Requirements

While the real time control system is required to run at 10 kHz, the VIRGO data acquisition system has been designed to operate at the maximum sampling frequency of 20 kHz in order to cover the usefull frequency range. It handles 5 Mbytes of continuous data per second with bursts at 10 Mbytes/s. It synchronises on the GPS based signals delivered by the Timing system. The Data Acquisition system implements a distributed readout system with high rate data transfer capabilities and long distance point to point communications between buildings all over the site.

Data taking operates as a continuous process which acquires data from various channels sampled at different frequencies. The DAQ system assumes VIRGO raw data collection, structures data into proper sets of information and distributes proper sets of information called frames to raw data archiving and online processing tasks [3].

B. Data Format

The frame format [4],[5] is provided as a common online and offline data format and has become a standard used now by the LIGO experiment [6]. A frame is defined as a data set of a few seconds length containing all the necessary information for the understanding of the interferometer over this time interval.

C. System Architecture

The Data Acquisition system is broken down into components according to its primary functions. As shown on Figure 5, the data sampled at high rates are collected by fast readout units and structured into frames by Local Frame builders.

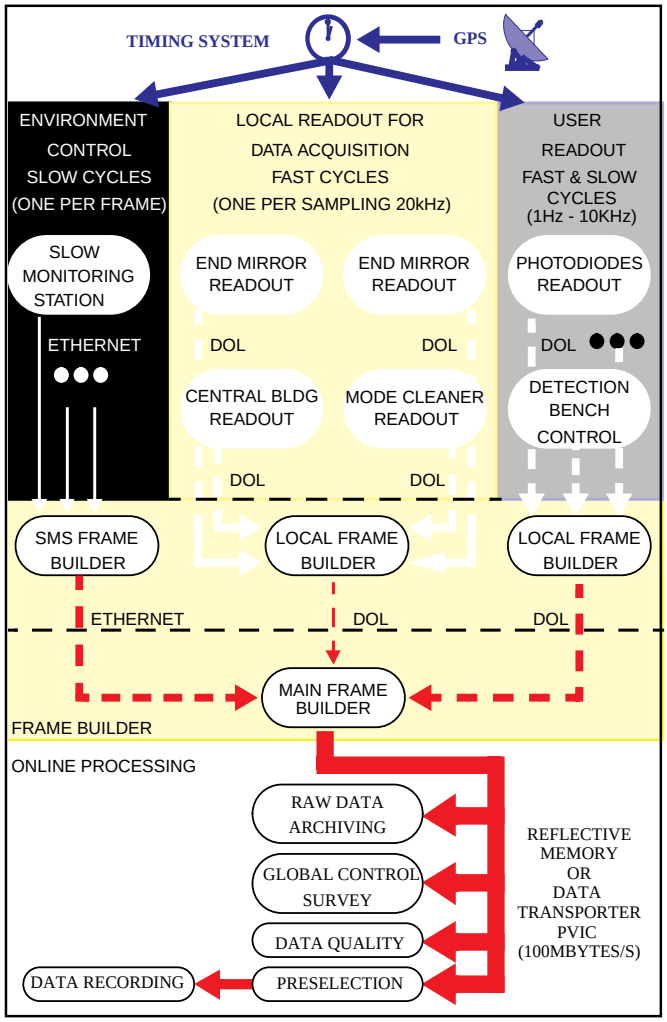

Figure 5: The Virgo data acquisition system

Data collection is supplied by the User Readouts and Local Readouts. The so-called User Readouts (e.g. the detection bench readout) contribute to the VIRGO Control System in so far as the concerned data are used by local controls before being passed to DAQ. In each building, a Local Readout unit collects the available data. Slow Monitoring information is passed to the DAQ system through the SMS frame builder interface. The Main Frame Builder combines data frames from the local stage and is in charge of frame distribution to raw data archiving and online processing tasks.

IV. Local Readout Unit

A. Hardware Components

The Local Readout unit is the DAQ front end component. Figure 6 provides a detailed view of the components which make up a typical readout crate. A Local Readout crate is controlled by a Power PC based RISC I/O board running the LynxOS real time operating system. The RIO2 8061 processor board from CES [7] has been selected considering interrupt handling capabilities and VME access performances [8]. 8µs has been measured as the typical value of the interrupt dispatch time under LynxOs (worst case around 20 µs) .

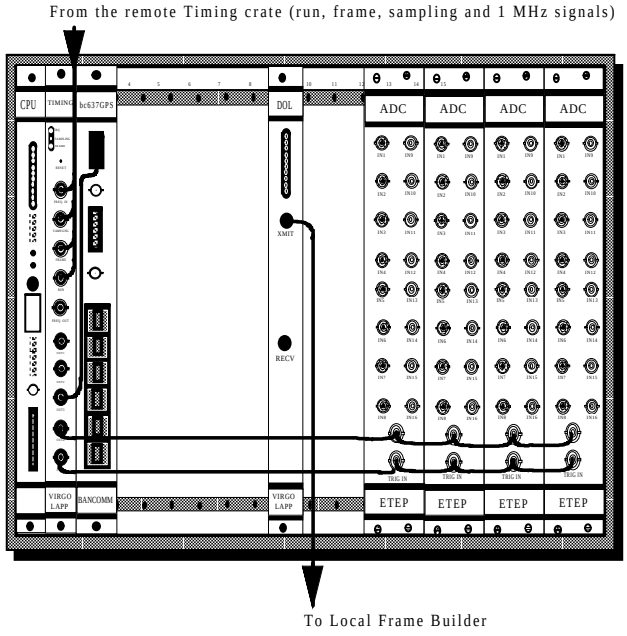

Figure 6: Readout crate

The clocking signals are distributed by the VIRGO Timing system [9] over optical fiber links. The local Timing board receives the signals, converts them to TTL, performs the sampling and frame counting and generates the VME bus interrupt for local use. Each sample is tagged using the Global Positioning System (GPS). The time stamp is delivered on demand by the bc635 VME Time and frequency processor from BANCOMM [10].

The Digital Optical Link (DOL) board [11] enables optical fiber connection with the Local Frame builder crate housed in the main building. Each DOL board has two channels, one for incoming data and one for outgoing data. Both channels are equipped with a 32 bit FIFO (depth : up to 16 kwords) which takes care of asynchronous operations between the optical link and the onboard local bus. Both the optical transmitter and receiver (DLT and DLR 1040 from Hewlett Packard) allow a transmission speed of 165 Mbits/s. The maximum parallel throughout achieved with a local oscillator of 15 MHz is 135 Mbits/s. A parity bit is generated for each data byte transmitted. DOL board may operate in write posting or in full duplex mode. It is housed in a VME/VSB module providing A24 A32 D32 BLT32 slave VME access.

The ADC board selected by the VIRGO collaboration is manufactured by ETEP company [12]. It has the following specifications: 16 individual and differential inputs, 16 bit ADC, user selectable input range: +/- 5V or +/- 10V, sampling frequency up to 40 kHz, onboard flip-flop memory, A32 D32 BLT32 slave VME data readout, and external trigger inputs. Due to the high dynamic of the signal, the photodiodes readout requires an effective 16 bit A /D converter. A dedicated board based on the 18 bit low noise 5020 ADC from Analogic has been developed [13].

B. Operational Overview

This section is intented to give an overview of the way a readout unit operates. Data flow is shown on Figure 7.

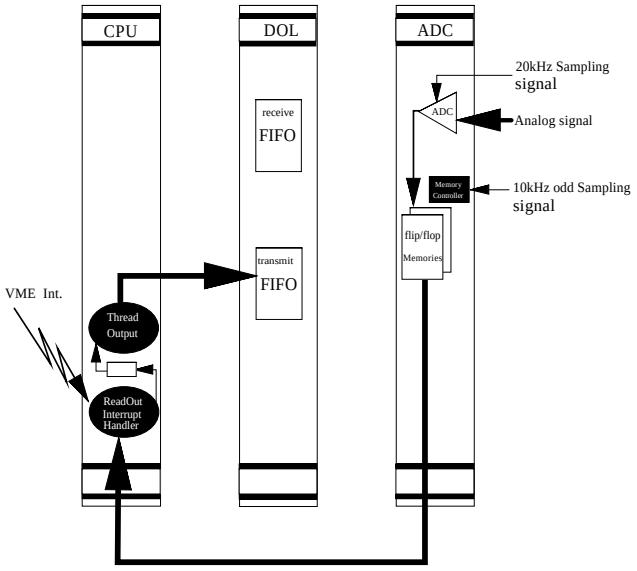

Figure 7: Local Readout data flow

During data acquisition, the 20 kHz sampling signal is received by the Timing board and routed to the ADC modules which perform continuous digitization at the supplied clock frequency of 20 kHz. An onboard FIFO allows the data readout at 10 kHz. Each ADC sample is stored in the onboard flip-flop memory which is controlled by the odd sampling signal. This buffer may handle several samples ready for readout. In coincidence with the odd sampling signal, the 10 kHz VME interrupt dedicated to the data acquisition process is generated by the Timing board. At this point, the VME interrupt is detected by an Interrupt Service Routine (ISR) in the CPU. The readout process reads data from the ADC modules into one of the two memory planes while they continue to digitize and store new data into the second plane of their flip-flop memories. This is done in Block Transfer (BLT). Data are then formatted and written into the FIFO memory situated on the DOL module which is ready to transfer data words. The transmission time over DOL is then hidden by the BLT VME transfer time. Readout operations are handled before the receipt of the next 10 kHz interrupt signal.

C. Software Organization

The Local Readout software combines real time tasks ensuring high speed data acquisition and numerical calculations with other processes handling user interface dialog and networking. A Local Readout control process will be implemented in LynxOS User Space, acting as the local server and driven by remote clients over TCP /IP sockets. An efficient implementation of Interrupt handling in device driver guarantees the interrupt response time. Deadline scheduling for critical readout operations is implemented in the kernel space, using kernel threads in order to off-load processing performed by interrupt routines and keep the overal real-time performance. The needs for numerical calculations is an important factor as well. Within 100 microseconds, lightweight processing such as data statistics or averaging may also be performed. We are currently investigating the way a digital filter including floating point operations could be applied at the kernel level. This implies restoring floating point mode of the Power PC processor which is disabled by LynxOS at the kernel level. Preliminary results obtained seem encouraging.

V. Frame Builder and Frame Distribution

Several Local Frame Builders receive in parallel the streams of data sent by the Local Readout units using DOL. These data are organized in frames as described in section III.*B*. No loss data compression is performed at that time. Then, the Main Frame Builder collects these frames using DOL links. They are grouped into a single frame which is distributed to the raw data archiving and the online processing tasks.

Reflective memories network may seem well-adapted to the problem of distributing frames to several computers. In fact, the required memory size of 32 Mbytes in order to handle one frame (e.g. 3s of VIRGO raw data) makes this technology quite expensive. Today, classical networks are at the edge of our requirement. The global PCI to PCI link (PVIC) announced by CES could be a solution. It acts more like a data transporter and provides transparent memory mapped connections running at full PCI speed (132 Mbytes bandwith) which correspond to 100 Mbytes/s sustained data channels. PVIC interfaces will be available under three form factors :VME 6U module, PCI Mezzanine Card (PMC) for in-crate processor, and PCI ISA for PCI-equipped workstations.

VI. Conclusion

The VIRGO Data acquisition which has been described is currently being developed in Napoli and Annecy. Real-Time readout and digital control systems running at 10 kHz have been designed making extensive use of commercial boards and LynxOS capabilities. The software developments are steadily going on. The mid term efforts should concern the integration phase which will start in 1998.

VII. Acknowledgments

We acknowledge the VIRGO Collaboration for many helpful discussions and suggestions.

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