Journal of Physics: Conference Series **122** (2008) 012011 doi:10.1088/1742-6596/122/1/012011

Application of a hybrid modular acquisition system to the control of a suspended interferometer with electrostatic actuators

F Acernese[1,2], F Barone[1,2], A Boiano[1], R De Rosa[1,3], F Garufi[1,3], L Milano[1,3], S Mosca[1,3], A Perreca[4], G Persichetti[1,3], R Romano[1,2]

[1]INFN - Sezione di Napoli, Complesso Universitario di Monte S.Angelo, via Cintia, 80126, Napoli - Italy
[2]Universitá di Salerno, via Ponte Don Melillo, 84084, Salerno - Italy
[3]Universitá di Napoli "Federico II", Complesso Universitario di Monte S.Angelo, via Cintia, 80126, Napoli - Italy
[4]University of Birmingham, Edgbaston, Birmingham, B15 2TT - UK

E-mail: fabrizio.barone@na.infn.it

Abstract. In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype developed for the implementation of distributed monitoring and control systems. The system, an alternative to the VME-UDP/IP based system, is based on a dual-channel 18-bit low noise ADC and 16-bit DAC module at 800 kHz, managed by an ALTERA FPGA. Experimental tests have demonstrated that this architecture allows the implementation of distributed control systems with delay time $t < 30\mu s$, on single channel, using a standard laptop PC for the real-time computation. The system was used for the longitudinal control of the end mirror of a suspended Michelson Interferometer, performed through an electrostatic actuators, giving effective performances. The preliminary results are also reported.

1. Introduction

The design and implementation of digital control systems, both for industrial application and for R& D experiments, needs a clear definition of the requirements on the sampling frequency, computing power, ADC and DAC characteristics. The implementation may often not be a particular problem, since many very reliable solutions and products exist on the market. The problem arises when the generation of the control signal requires large computing powers, especially when the control bands are of the order of some kHz. To overcome the problem of the control computing power, an efficient and, nowadays, standard solution is that of using Digital Signal Processors (DSP) integrated in the acquisition and control system. This is what is currently done, for example, in the control system of the Interferometric Detector of Gravitational Waves Virgo [1], where DSP based on VME architecture have been specifically designed and implemented to satisfy the requirement on computing power of the detector control system. Nonetheless, this solution is expensive and not versatile for small experiments, remote sensors, embedded systems or, simply, for R&D experiments.

A few years ago we decided to explore new possible directions of research privileging the

implementation of efficient, standardized, low cost, high computing power and versatile digital control systems. We started from the idea that what is really important in the implementation of a digital control system is the basic principle on which the system is implemented, that is the synchronous link among the units. The data transfer and the computing power must allow the designed control frequency, f_c to be sustained. The idea is to have the acquisition/actuation units linked to the computing unit through standard asynchronous protocols. It seems to conflict with the obvious requirement of control systems, i.e. a synchronous link among the units. This constraint can be overcome if the asynchronous data transfer is so fast that the sampling frequency of the control system is statistically guaranteed, to consider the link as synchronous from the point of view of control theory. In the following we will refer to this class of control systems as *Hybrid Acquisition and Control Systems*. As a consequence we began a study to test different technical configurations suitable for the implementation of such kind fo control system [2], aiming to demonstrate the feasibility of hybrid control systems with sustained sampling frequencies, f_c, of the order of 100 kHz.

In this framework, we developed a modular board with a 18 bit Successive Approximation (SAR) ADC, a 16 bit DAC and a communication channel that allows to connect the board to the standard I/O ports available on present day PCs without the need to use a specifically designed solution, capable to achieve a control frequency band up to tens of kHz. Actually, the complete project foresees the implementation of a modular ADC/DAC card to be assembled in up to six copies on a single motherboard [3], that should host the default link, the main processor and a bus where the ADC/DAC modules can be connected. The implementation of the motherboard is not yet started and deferred to the completion of the final tests we are performing on the suspension control of the interferometer prototype. The first prototype of the ADC/DAC module has been designed, prototyped and tested, connected with a specifically designed interface to a NIOS development kit [4] used as a simulation of the motherboard. With this set-up we tested the behaviour of the hybrid acquisition and control system with Ethernet, RS232 and Enhanced Parallel Port (EPP - IEEE1284) connected to a PC [5]. The best results were obtained using a standard EPP, that allows to sustain a control frequency of ($f_c \approx 80\,kHz$), that is very close to our final goal.

In this paper we outline the architecture of the board and its performances, and describe the results of the implementation of this board for the control of a suspended Michelson interferometer by using an electrostatic actuation system on one of the suspended mirrors.

2. The Module Prototype

2.1. Concept and implementation

We have developed a board that integrates all the functionalities of the acquisition and control unit. This board is based on the Cyclone® (or Stratix®) family of Altera Programmable Logic Devices (PLD) and has been developed with the help of the NIOS II® [4] development kit, an integrated board providing a hardware platform for developing embedded systems based on Altera® Cyclone II devices.

At present we developed only a prototype daughterboard hosting two independent channels. The daughterboard (see Fig. 1) has a Cyclone EP1C6F256C6 FPGA, two ±10 V differential input and two differential ±10 V outputs on a load of 1 kΩ.

Each channel contains a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545), a 20 bit DAC (Burr-Brown DAC1220) and a 14 bit ADC. The two 16 bit DACs in each channel have different purposes in the input and output paths. In the input path section A is used as Programmable Gain Amplifier (PGA) and section B to set the offset of the 18 bit ADC, while in the output path selection A sets the gain of the output channel, while section B sets the output. This implies that the same board channel cannot be used at the same time as fast input and output channel. Each channel can, instead, be used either as a *fast* 16 bit DAC with a settling time

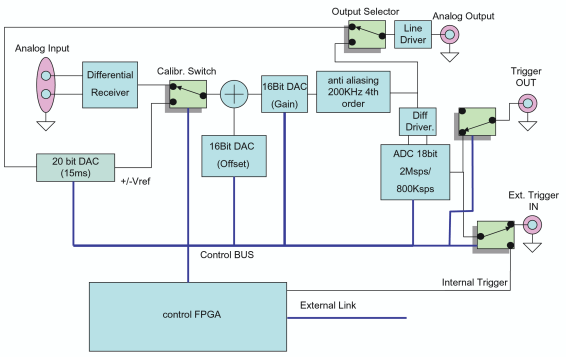

Figure 1. ADC/DAC Module input channel schematics. The switches connected to the control bus are managed by FPGA registers, the output selector is set via a jumper. The ADC trigger can be either internally generated or external and, in both cases can be routed to an output connector.

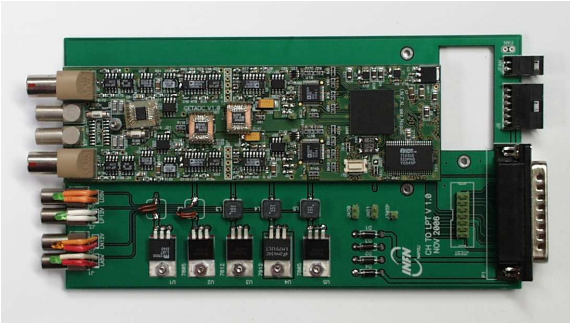

Figure 2. The Prototype of the Module in standalone configuration with the power distribution board. The hole in the power distribution base is to host the fan.

of $0.5\,\mu s$ or as a 18 bit ADC with a maximum theoretical conversion rate of $2\,Msamples/s$ (for the first prototype a $800\,kHz$ ADC is used). Alternatively each channel can be used as a 18 bit ADC and, at the same time, a (slow) 20 bit DAC with a settling time of $2\,ms$. The ADC trigger signal can be either internally generated on the motherboard or daughterboard PLD or taken from an external signal; both the internally generated and the external trigger pulses can be routed on an output connector. An analogic 4^{th} order anti-aliasing filter is placed both on the input and the output path. The 14 bit DAC is used to read the board temperature to provide an eventual on-line correction.

2.2. Performance Tests

The first prototype, realized to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency.

The NIOS kit was programmed in C language by means of the Altera Quartus II® development software. The PLD on board the module was not used at all.

The data stream to the PC is composed by a sequence of 3 words of 32 bit per ADC sample: the first 2 words represent an internally generated time tag and the third the ADC data. By reading the data FIFO register at the maximum speed allowed by the communication link and looking at the most significant bit the last converted data is read at the maximum speed.

With this prototype, we performed tests on the ADC performance and on different communication links. The first tests we performed were aimed to evaluate the performances of the Fast Ethernet solution. The tests produced very unsatisfactory results showing a slower link speed with respect to the tests performed on a VME board used in the feasibility phase [3]. Therefore, we decided to test different communications links, that are the on board RS232 serial port and the Enhanced Parallel Port (EPP). In this and the successive tests, the whole acquisition-transmission-actuation loop has been evaluated, performing integrated tests, as discussed in the next paragraph.

2.2.1. Integrated tests. The complete signal round-trip by using a Linux laptop with a Intel Centrino 1.8 GHz CPU as computing unit, connected with a RS232 port, has given a maximum

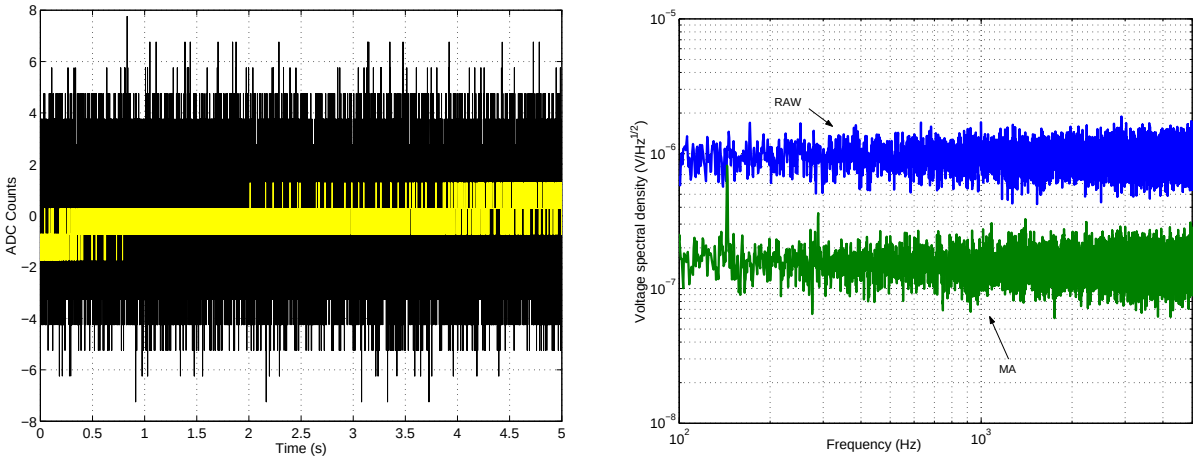

Figure 3. Internal noise acquired at 10 kHz (a) raw and filtered with the Moving Average and (b) power spectral density of the two data series. The Moving Average operation lowers the noise level of a factor ~ 10 at this frequency (1 count $= 20/2^{18}$ V).

sampling frequency of 1.25 kHz. The ADC sampling clock pulse used in this test has been both internally and externally generated, with no substantial difference.

Then the NIOS kit FPGA has been programmed in VHDL to use some output pins to manage a protocol compatible with an Enhanced Parallel Port (EPP) on a personal computer. Finally, the ADC-DAC module has been tested standalone, without the help of the NIOS kit, and using a parallel port as communication link.

The PLD on board the module has been programmed in VHDL in order to manage a protocol over an EPP Parallel Port, that allows programming and reading the internal module registers from the remote PC. For these tests, a power distribution board hosting the parallel port D25 connector, low noise voltage regulators, the data and power lines has been designed. The C language program used to program the NIOS development kit has been adapted to use the EPP protocol from a linux PC. This solution allows to drive only one module per parallel port. A picture of the module in standalone configuration is shown in Fig. 2. With this setup we again tested the complete signal round-trip, obtaining a maximum sustained sampling frequency of $\sim 40\,kHz$, although frequencies up to $\sim 80\,kHz$ were reached when the time tag information was not enabled nor transmitted with data.

2.2.2. Noise and on board filter tests. The VHDL program used in this new *standalone* architecture gives also the possibility of acquiring samples at the maximum ADC speed and of decimating the samples synchronously to an external trigger. To this purpose we developed on the board a digital moving average (MA) filter whose output is the average of the samples acquired between two trigger pulses. In this way the same VHDL filter implementation can be used with any trigger frequency allowed by the communication link, while a more complicated filter would have required different numeric parameters for different frequencies.

To characterize the electronic and acquisition noises of the ADC, we acquired some seconds of data with the input closed on a 50 Ω termination, with and without the MA filter at different acquisition frequencies. Without the MA, we noticed a 10 LSB wide noise, while with the MA the *internal* noise is reduced to 2–3 LSB over the observed period at frequencies of 10 kHz, as can be seen in Fig. 3.

3. Application to a Suspended Interferometer

The digital board functionality, apart from the performances tests developed in the first phase, was proved by using it in the digital control of one of the suspended mirror in a short suspended Michelson interferometer.

3.1. Experimental setup

The interferometer was realized by using two suspension systems, for vibration isolation purposes, that were placed on a standard optical bench. Each suspension was composed by two suspended stage. The first stage, that was similar for both the suspensions, was equipped with coil-magnet pairs for the actuation and optical levers for the position monitoring and was suspended, by means of a single stainless steel wire, to the hosting structure. The second stage was different for each suspension. For the first suspension it consisted of a small bench that was used to hold the beam splitter and one of the arms of the interferometer, that was folded to fit the available space. For the second suspension it consisted of a single dielectric cylindrical mass with a small mirror in the front, that constituted the end mirror of the second arm of the interferometer. No direct actuation system was provided for the suspended bench, while an electrostatic actuator, fixed on the optical bench, was used for the fine control of the mirror. All the system was placed in air and both the laser and the output photodiode were fixed on the optical bench.

As source a frequency stabilized, 1.5 mW, HeNe laser was used, while for the optical lever very simple laser diodes, emitting 3 mW at 680 nm were employed. The optical levers were realized by using a simple setup: by fixing a mirror on the first suspended mass, that steered the beam coming from the source on a lens followed by a beam splitter. The outcoming beams were collected by two position sensing photodiodes, placed at suitable distances from the lens. In this way it is possible to uncouple the angular displacements from the longitudinal one [6].

The actuator for the mirror consisted of a set of 4 patterns of electrostatic actuator, realized on a standard electronic grade substrate. The geometry allowed to move the mirror along the optical axis as well as to rotate it around the two other axis. Each pattern consisted of 8 electrodes, 4 mm large and 4 cm long. The distance between the electrodes was 1 mm, that is the same value of the distance between the actuator and the suspended mass. The geometrical parameters of the each actuator pattern were chosen both on the basis of the available space and of a numerical model [7]. A scheme of the interferometer is drawn in Fig. 4

3.2. The Control System

The control of the interferometer was, conceptually and practically, divided in two part. The first issue was the damping and the positioning of the suspended elements, namely the bench and the mirror. This was performed by using a VME based digital control system, able to manage the high number of analog inputs coming from the optical sensing system of the two suspensions. Once the damping was performed, the interferometer was manually aligned by acting on the reference values of the control loops, in order to maximize the contrast.

The second step was the locking of the interferometer, fulfilled by acting on the suspended dielectric mass by the electrostatic actuator. Since this actuator can only attract the mass, a bias was used in the correction signal in order to be able to perform correction on both directions. Moreover, since the stray electrical charges present on the mass produce an extra force on the mass itself, a alternate voltage bias instead of a continuous one was employed. The interference signal around its mean value was used as error signal and the interferometer was locked on the half fringe. The alternate bias was digitally produced using the ADC/DAC board, connected to a standard PC, and consisted of a 800 Hz sinusoidal wave. The sampling frequency was fixed to 10 kHz. Of course this system was also used to compute the correction signal from the interference signal. The set-up worked effectively, as shown in Fig. 5, where a comparison of the

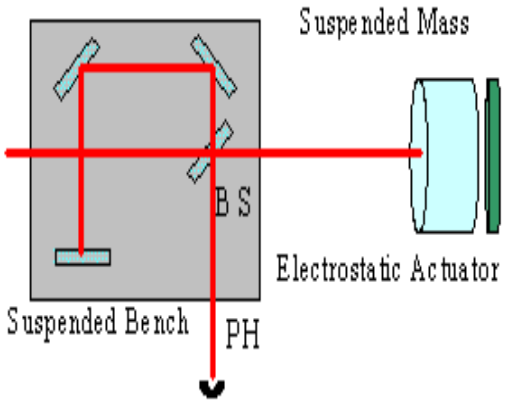

Figure 4. Basic scheme of the suspended interferometer

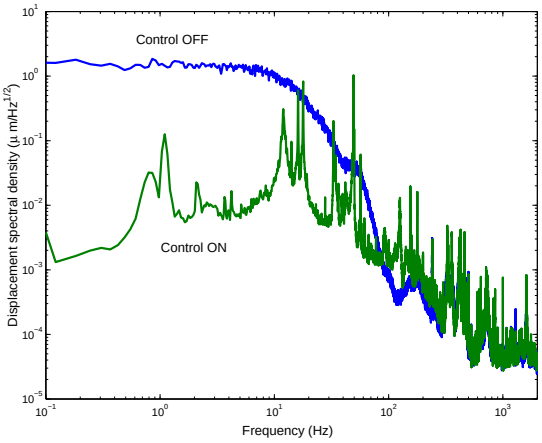

Figure 5. Displacement spectral density of the residual relative motion between the interferometer arms.

residual relative displacement between the arms, in open and closed loop condition, is reported. The slight displacement noise excess between 100 and 200 Hz is due to the large frequency band of the control loop that reintroduce control noise inside the interferometer. An improved control filter, with stronger roll off close to the unity gain frequency should overcome this problem, but its implementation, that also requires some change to the analog electronic used to drive the electrostatic actuator, was postponed for the next upgrade.

4. Conclusions

In this paper we demonstrated the effective performances of a ADC/DAC board, designed for data acquisition and control purposes, that can be managed by using simple and commercially available computing systems, like standard PCś or even laptops. The board was equipped with standard antialiasing filters and has small real time data processing capabilities to enhance the signal resolution by oversampling and averaging techniques. The effective performances of the board were tested by using it as the main element of the control loop in a suspended Michelson interferometer, by controlling the mirror displacement by means of an electrostatic actuator. The good results obtained allow us to consider future upgrades, mainly in terms of available channels on the single board.

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