Hybrid control and acquisition system for remote control systems for environmental monitoring

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ABSTRACT

In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype for environmental monitoring and geophysics. The system, an alternative to a VME-UDP/IP based system, is based on a dual-channel 18-bit low noise ADC and a 16-bit DAC module at 1 MHz. The module can be configured as stand-alone or mounted on a motherboard as mezzanine. Both the modules and the motherboard can send/receive the configuration and the acquired/correction data for control through a standard EPP parallel port to a standard PC for the real-time computation. The tests have demonstrated that a distributed control systems based on this architecture exhibits a delay time of less than 25 us on a single channel, i.e a sustained sampling frequency of more than 40 kHz (and up to 80 kHz). The system is now under extensive test in the remote controls of seismic sensors (to simulate a geophysics networks of sensors) of a large baseline suspended Michelson interferometer.

Keywords: Hybrid Control, Data acquisition, Remote Control

1. INTRODUCTION

Automatic control systems may require computing powers often quite difficult to be provided by embedded systems. In fact, distributed control systems are often characterized by many inputs and outputs, so that the necessary computing power for control signal generation may be quite high and it can be difficult to sustain the chosen sampling frequency, f_c. To overcome the problem of the control computing power, an efficient and, nowadays, standard solution is that of using Digital Signal Processors (DSP) integrated in the acquisition and control system. This is what is currently done, for example, in the control system of the Interferometric Detector of Gravitational Waves Virgo.[1] Nonetheless, although very efficient, this solution may be expensive and not versatile for small experiments, remote sensors, embedded systems or, simply, for R&D experiments. Therefore, a few years ago we decided to explore new possible directions of research in designing standard, low cost, high computing power and versatile digital control systems. The starting point of our approach is the requirement for a digital control system of a synchronous link among the different units (ADC, CPU and DAC). Actually, this requirement does not put any restriction on the protocol used for data transfer (synchronous or asynchronous) or on the operating system of the CPU, but states that all the operations of data transfer (ADC/CPU and CPU/DAC) and data processing must be always performed by the system in a time shorter than $t_c = 1/f_c$, where f_c is the digital control system sampling frequency. Therefore, it is, in principle, possible to link the acquisition/actuation units with the computing unit through standard commercial asynchronous protocols. This solution seems to conflict with the *classical* requirement of a synchronous link among the units. Nonetheless, if the asynchronous data transfer is so fast that the sampling frequency is statistically guaranteed, then also an asynchronous link can be considered *synchronous* from the point of view of control theory. The advantage of

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this architecture is that the computing unit is completely independent from the acquisition/actuation unit, and, therefore, the computing unit can be chosen among a large variety of powerful and cheap standard technical solutions available on the market. In particular, the acquisition/actuation unit can be also a remote low-power system, equipped with a suitable link and a transmission protocol on board for connection with the computing unit. Of course, this configuration still allows the use of the standard oversampling techniques for input digital noise reduction but its great advantage is that the computing power unit can be defined and chosen in a completely independent way from the acquisition/actuation unit.

In 2003 we began to study and test different technical configurations, aiming to demonstrate the feasibility of hybrid control systems with sustained sampling frequencies, f_c, of the order of 100 kHz.[2] This is the requirement on the digital control sampling frequency of a prototype of suspended optical interferometer we are developing at the INFN - Napoli for R&D on the second generation of interferometric detectors for gravitational waves, that is $f_c = 10$ kHz (the same frequency of the Virgo control system).

The implementation of a hybrid control system requires the choice of acquisition/actuation units with suitable communication channels. Many ADC/DAC boards are available on the market for the vibration monitoring and suppression (see e.g.[3,4]), but not suitable for our purposes because of the ADC and DAC limited resolution and the lack of a standard communication link, being conceived to work together with DSP boards or inside a PC or make use of $\Sigma - \Delta$ ADCs that are not suitable to follow slowly variable signals, as, e.g., the interferometer suspensions' oscillations, mareal accelerations, or slow deformations. For this reason we developed a modular board with a 18 bit Successive Approximation (SAR) ADC, a 16 bit DAC and a communication channel that permits to connect the board to the standard I/O ports available on present day PCs without the need of using a specifically designed solution and capable to achieve a control frequency band up to tens of kHz. The complete project foresees the implementation of a modular ADC/DAC card to be assembled in up to six copies on a single motherboard,[6] hosting the default link, the main processor and a bus where the ADC/DAC modules can be connected. Both a channel identifier and a time tag can be encoded with each ADC sample and sent to the control PC. The implementation of the motherboard has be postponed to the completion of the tests we are performing on the suspension control of the optical interferometer prototype in Napoli.

The first prototype of the ADC/DAC module has been designed, prototyped and tested, connected with a specifically designed interface to a NIOS development kit[7] used as a simulation of the motherboard. With this set-up we tested the behaviour of the hybrid acquisition and control system with Ethernet, RS232 and Enhanced Parallel Port (EPP - IEEE1284) connected to a PC.[8,9] The best results were obtained using a standard EPP, capable to sustain a control frequency of ($f_c \approx 80$ kHz), that is very close to our final goal.

We also considered the possibility of using the ADC/DAC module without an intelligent motherboard. For this purpose, the communication logic has been embedded in the module's FPGA, and the module itself has been tested standalone in connection with a PC through a standard EPP.

In this paper we discuss the architecture, the configuration, the performances and the applications of this hybrid digital control system.

2. PRELIMINARY STUDIES

2.1 The Model

In the following we will describe the model we used to demonstrate the theoretical feasibility of a hybrid digital control system. If we define the Data Acquisition Time (ADC and DAC data conversion times), T_{DC}, the Data Transfer Time, T_{DT} and the Data Processing Time, T_{DP}, then the time T_{DM} necessary to generate the control signals from the input analog signals, is:

$$T_{DM} = T_{DC} + 2 \cdot T_{DT} + T_{DP} < 1/f_c \tag{1}$$

where f_c is the sampling frequency (i.e. the loop *control* frequency), which defines the maximum control band, B, of the system (typically $B < f_c/10$), assuming a symmetrical communication link and the same amount of data in both directions. The T_{DM} parameter can be easily measured through a simple application test: a known signal (e.g. a sine wave) with a fixed sampling frequency, f_c, is digitized by the ADC and sent through the link

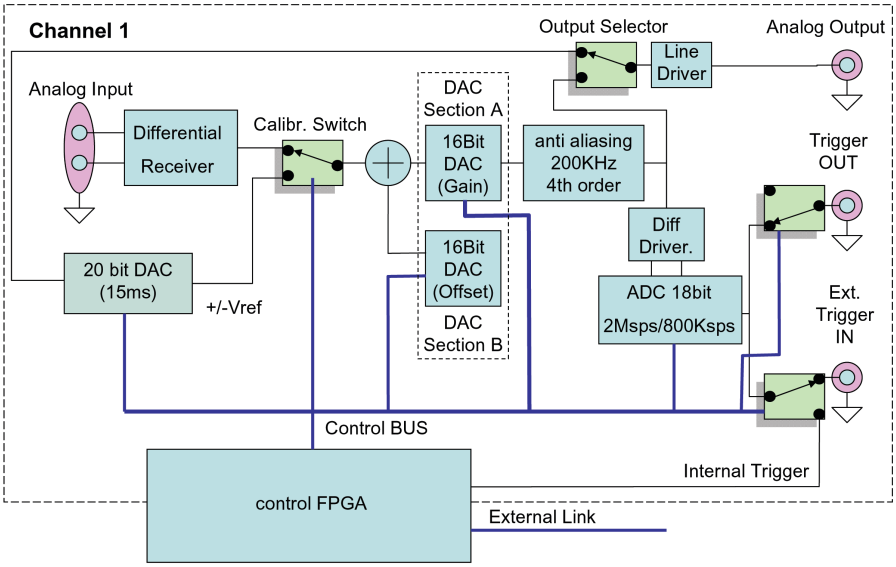


Figure 1. Block scheme of the acquisition and control daughterboard. In the picture only one channel is shown, being everything but the FPGA duplicated for the other channel. The switches connected to the control bus are managed by FPGA registers, the output selector is set via a jumper. The ADC trigger can be either internally or external generated and, in both cases, can be routed to an output connector.

to the computing unit; the latter simply sends it back to the DAC, that converts it again to an analogic signal. The input signal and the output signal are observed with an oscilloscope. It is easy to see that in this test $T_{DP} = 0$ s, so that the measured quantity is the Round Trip Time, $RTT = T_{DC} + 2 \cdot T_{DT}$, i.e. the time the whole system takes to convert, transfer through the chosen link technology and convert back the data. The quantity T_{DP}, depends mainly on the available computing power and on the complexity of the real-time computation; nonetheless, taking into account the very high computing power of the state-of-the-art computing units, it can be considered negligible with respect to T_{DC} and T_{DT} in most cases. On the other end, the quantity $2 \cdot T_{DT}$, can be evaluated independently with a network-only test where a packet is generated in the acquisition unit, sent to the computing unit and sent back to the acquisition unit.

2.2 Preliminary Tests

The first general tests on the hybrid architecture were performed with an VME-UDP/IP based system, derived from an already existing system originally used for developing software for tests on digital control systems for a VIRGO R&D program.[2,6] The goal was to replicate the performance of the existing system with the new architecture. The first tests performed with this VME-UDP/IP setup have been just the simple acquisition-actuation round-trip described in the previous subsection and have shown a control signal delay of ≈ 2 samples at a maximum sampling frequency of 6.2 kHz[2,6] although the simple UDP packet round-trip test gave times in the 240 μs range. Since the result on the acquisition-actuation test was quite far from our goal of $f_c = 100$ kHz, we decided to replicate the network based tests on the module prototype and to test different protocols.

We will describe the architecture and the results in the following sections.

3. THE MODULE PROTOTYPE

3.1 Concept and Implementation

In order to make the hybrid acquisition and control useful for field applications, we have designed a daughter-board prototype, integrating all the functionalities of an acquisition and control unit. The board, based on the Cyclone® family of Altera Programmable Logic Devices (PLD), has been developed with the help of the NIOS II® development kit,[7] an integrated board providing a hardware platform for developing embedded systems based on Altera® Cyclone II devices, providing also an on-board Ethernet interface and RS-232 serial port.

While the full project would consist of a motherboard hosting multiple copies of the acquisition and control daughterboard, we are currently working only on the prototype of daughterboard. The daughterboard prototype (see Fig. 1) hosts a Cyclone FPGA and two independent channels ($\pm$10 V differential input - differential $\pm$10 V outputs on a load of 1 kΩ). Each channel consists of a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545), a 20 bit DAC (Burr-Brown DAC1220). The two 16 bit DACs (called Section A and Section B) have different purposes in the input and output paths. In the input path, Section A is used as Programmable Gain Amplifier (PGA) and Section B is used to set the offset of the 18 bit ADC, while in the output path Section A is used to set the output channel gain, while Section B is used to set the output. This implies that a channel can be used as either an input channel or as an output one. Each channel can be used instead either as a *fast* 16 bit DAC with a settling time of 0.5 μs or as a 18 bit ADC with a maximum theoretical conversion rate of 2 Msamples/s (for the first prototype a 800 kHz ADC is used). Alternatively each channel can be used as a 18 bit ADC and, at the same time, a (slow) 20 bit DAC with a settling time of 2 ms. The ADC trigger signal can be either internally generated on the motherboard or daughterboard PLD or taken from an external signal: both the internally generated and the external trigger pulses can be routed to an output connector. An analogic 4^{th} order anti-aliasing filter is placed both in the input and the output path. A 14 bit ADC (internal to AD7641) is used to read the board temperature for on-line correction.

Mechanically, the module is conformant to a 2U Eurocard with a connector providing the interface with the motherboard and/or to a power supply and external link board.

3.2 Performance Tests

The first prototype, realized to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency. The NIOS kit was programmed in C language by means of the Altera© Quartus II® development software. The PLD on board the module was not used at all.

With this prototype, we performed tests on the ADC performance and on different communication links to demonstrate the feasibility of the whole architecture.

3.2.1 ADC Performances

The purpose of the tests on ADC we performed is only to verify at this state the correct functioning of the board and to have a rough idea of the ADC resolution.

To test the ADC, we simply acquired a sine wave with a 1 kHz frequency and 50 mV or 120 mV peak to peak amplitude. A simple program on the NIOS, allowed the acquisition in memory of 1 s of data and then transmit them to the PC through the RS232. We then evaluated the residuals of a fit with a sine function. The results at 120 mV are shown in Fig. 2. A value of $\pm$6 ADC counts, both at 50 mV and 120 mV, results from the convolution of both the ADC and the generator precisions. Assuming 18 bits over a $\pm$10 V scale, this means a precision of $12 \times 20\ \mathrm{V}/2^{18} \sim 9.2 \times 10^{-4}$ V, although it should be a function of the sampling frequency and of the input signal slope.

3.2.2 Integrated tests

The complete signal round-trip test with a Linux laptop with a Intel Centrino 1.8 GHz CPU as computing unit, connected with a RS232 port, has given a maximum sampling frequency of 1.25 kHz. The ADC sampling clock pulse used in this test has been both internally and externally generated, with no substantial difference.

Then the ADC-DAC module has been finally tested standalone, without the help of the NIOS kit, and using a parallel port as communication link. The PLD on-board the module has been programmed in VHDL in order to manage a protocol over an Enhanced Parallel Port EPP, that allows programming and reading the internal module registers from the remote PC. For these tests, a power distribution board hosting the parallel port D25 connector, low noise voltage regulators and the data and power lines has been designed. The C language program used to program the NIOS development kit has been installed on the PC and adapted to use the EPP protocol. This solution allows to drive only one module per parallel port. A picture of the module is shown in Fig. 3. With this setup we again tested the complete signal round-trip, obtaining a maximum sustained sampling frequency

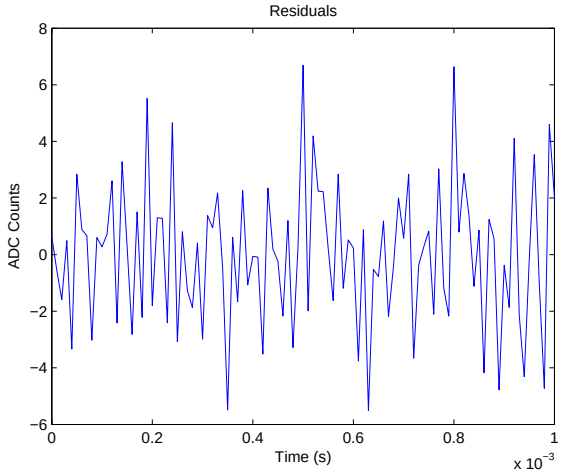


Figure 2. Difference between the ADC read value and the input sine wave for 120 mV amplitude. The input sine wave estimation is the result of a fit. The maximum value of the residual is a result of the sampling step and the input signal slope.

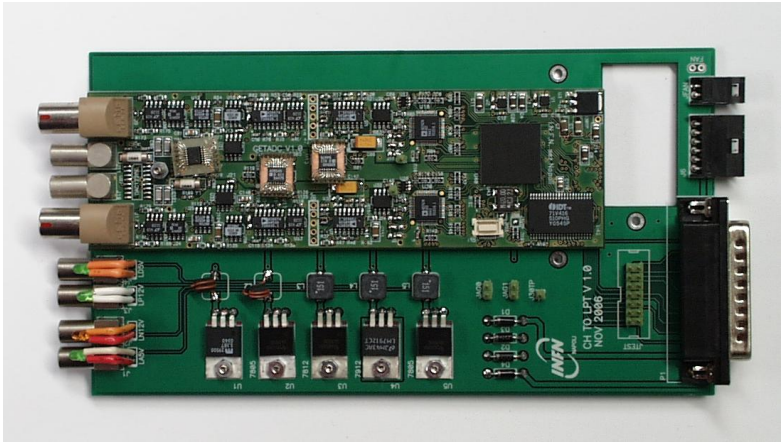


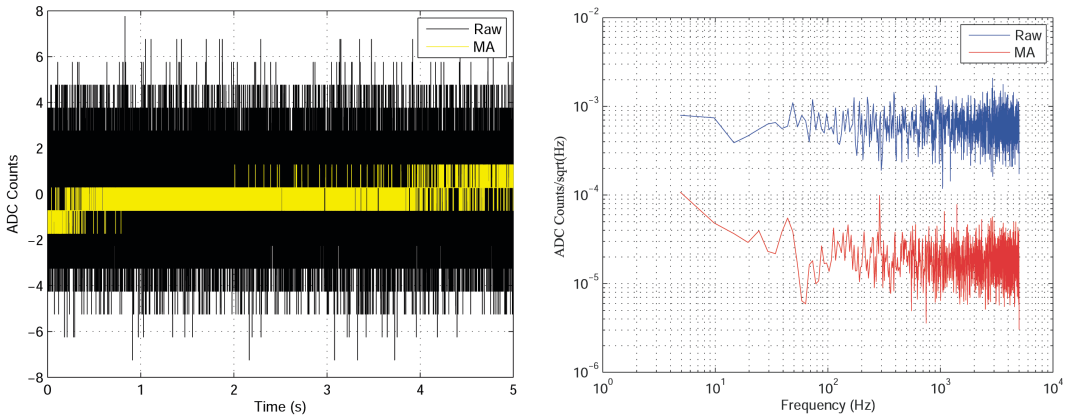
Figure 3. The Prototype of the module with the power distribution board. The hole in the power distribution base is to host the fan.

of ~ 40 kHz, although frequencies up to ~ 80 kHz were reached when the time tag information was not enabled nor transmitted with data.

This new *standalone* architecture gives also the possibility of acquiring samples at the maximum speed allowed by the ADC and of and filling the data FIFO with the last acquired sample synchronously to an external trigger. To this purpose we developed on the board a digital moving average (MA) filter whose output is the average of the samples acquired between two trigger pulses, thus, for a trigger frequency of $10\,kHz$ and an ADC clock speed of $800\,kHz$, the acquired samples are the result of averaging $800/10 = 80$ ADC samples. In this way the same VHDL filter implementation can be used with any trigger frequency allowed by the communication link, while a more complicated filter would have required different numeric parameters for different frequencies.

To characterize the electronic and acquisition noises of the ADC, we acquired some seconds of data with the input closed on a $50\,\Omega$ termination, with and without the MA filter at different acquisition frequencies. Without the MA, we noticed a 10 LSB wide noise, while with the MA the *internal* noise is reduced to 2–3 LSB over the observed period at frequencies of 10 and $20\,kHz$, as can be seen in figure 4. In the same figure, it is possible to see a trend in the MA data, that can be interpreted as a temperature effect, as will be explained later in the paper.

A 14 bit ADC is available to read an on board temperature sensor. The temperature information can be



(a) (b)

Figure 4. (a) Internal noise acquired at 10 kHz raw and filtered with the Moving Average and (b) power spectral density of the two data series. The Moving Average operation lowers the noise level of a factor $\sim 10^2$ at this frequency (1 count $= 20\,V/2^{18}$).

acquired without the need of a trigger pulse. In this way it is possible to correct the 18 bit ADC data taking into account the temperature drifts, by periodically acquiring the temperature information.

To test the effects of the temperature on the board we acquired the *terminated* input channel at different temperatures, using a moving average with a sampling frequency of $200\,Hz$. We noticed that the ADC counts are not a linear function of the temperature change, although it can be considered linear in intervals of about $5°C$. The fits show that the temperature coefficient takes values in the interval from ~ 4.5 to ~ 6.5 $counts/°C$ in the range $40 - 55°C$. Being these results very encouraging we have implemented a new prototype board with a $2\,MHz$ ADC with the same architecture described here. The first tests on this prototype show that the ADC is more noisy than the $800\,kHz$ model. Although this is expected from the product data sheets, giving a SNR of *101 dB* for the *800 kHz* and *96 dB* for the *2 MHz*, the larger number of averages per sample allowed by the higher ADC clock speed is not enough to compensate the difference. All the other parameters seem to be unchanged.

The choice of parallel port as communication link has been dictated by the availability of the hardware on most of present day personal computers. To increase the bandwidth of the control system we are now studying other possible solutions based e.g. on optical fiber interfaces.

3.3 Applications

The system is being extensively tested in the control of a suspended Michelson interferferometer, a prototype of velocimeter for geophysical applications and for the development of control systems techniques for interferometric detectors of gravitational waves and. In particular, the control action under test is active only on one suspension, both at the suspension top stage, through mechanical accelerometers,[10] and at the lower stage, directly to the end mirror of the suspended Michelson Interferometer, through electrostatic actuators.[11] In fact, at the top stage, three monolithic tunable folded pendula, shaped with precision machining and electric-discharge-machining, are located in force-feedback configuration, acting as accelerometers. The monolithic mechanical design and the introduction of laser interferometric techniques for the readout implementation make it a very compact instrument, very sensitive in the low-frequency seismic noise band, with a very good immunity to environmental noises.[10] The hybrid control system is used here for providing the feedback action to the monolithic sensors so that they behave as accelerometers, and to acquire the data necessary for the measurements of the suspension top stage motion.

The hybrid system is then used for the control of the end mirror through electrostatic actuators.[11] The lower stage of the interferometer is shown in Fig 5. Both arms optics are mounted on the lower stages of double pendular suspensions, the upper stages and one lower stage being controlled by means of coil-magnet actuators. For both upper stages the digital control is achieved by using a standard VME ADC-CPU-DAC architecture. In one arm, the lower stage the mirror tilts are controlled with classical optical levers, consisting of laser and position

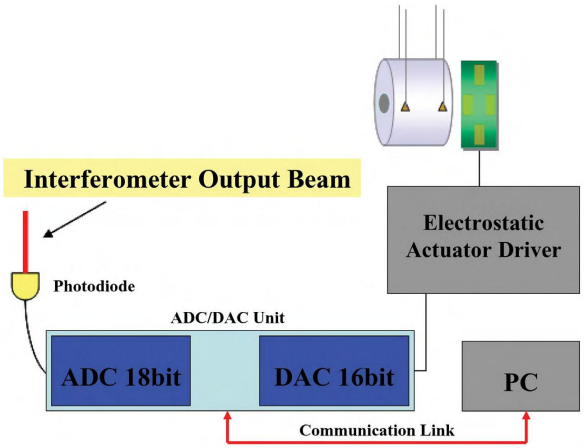


Figure 5. Lower stage of the suspended interferometer with read-out and control schematics.

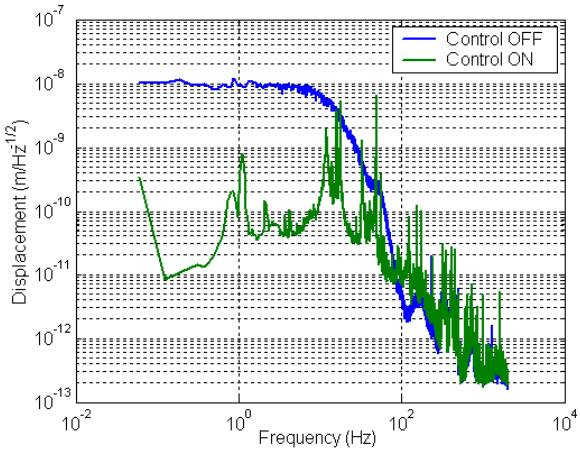


Figure 6. Preliminary results of the suspension lower stage control with electrostatic actuators. The power spectral density of mirrors' relative displacement are shown both with and without the lower stage control. The peaks in the controlled power spectrum are due to residual mechanical rotational-translational modes coupling and violin modes.

sensing diodes (PSD), while the mirror longitudinal motion is controlled, through electrostatic actuators, with the 18 bit hybrid digital control system. The lock of the interferometric system is easily achieved. Preliminary results displayed in Fig. 6 show that the control is capable of a reduction of two orders of magnitude in the mirror displacement noise in the mHz - 10 Hz frequency band, that is what we expected from the theoretical simulation of the control system.

Since the sampling frequency is much lower than the maximum frequency for each channel, it is possible to think to control many different channels of the interferometer with a single board. For this tack a multiplexing/demultiplexing scheme is in a design study phase. The different channels can be acquired in sequence by means of a "fast" multiplexer, and the control signal can be obtained by demultiplexing the output DAC signal with a delay of one (or two) trigger tick with respect to the input.

Finally, this board is used in Salerno to monitor the output of monolithic seismometers with interferometric read-out, to be used in a network of seismic sensors sensitive to a wide range of frequencies. In this application, due to the low acquisition frequency, more than a board can be acquired with a multi-parallel card on a PC.

4. CONCLUSIONS

We have designed and prototyped a hybrid acquisition and control system with an on-board communication link. This solution allows the collection of data into a control station and the actuation/tuning on the basis of the collected data. The preliminary tests have shown that the developed system can sustain a sampling frequency ranging from the mHz region up to $f_c > 40\,kHz$ with a standard protocol over an Enhanced Parallel Port (EPP) and can enhance its precision by using an oversampling/averaging filter. The system is now under extensive test in the control of a suspended Michelson interferferometer, that is a prototype designed for geophysical applications and for the development of control systems techniques for interferometric detectors of gravitational waves. In particular, the control action under test is active only on one suspension, both at the suspension top stage, through mechanical accelerometers,[9] and at the lower stage, directly to the end mirror of the suspended Michelson Interferometer, through electrostatic actuators.[11] Finally, this board is used in Salerno to monitor the output of a monolithic seismometer with interferometric read-out, to be used in a network of seismic sensors sensitive to a wide range of frequencies.

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