Hybrid control and acquisition system for distributed sensors for environmental monitoring

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ABSTRACT

In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype we developed in Napoli for the implementation of geographycally distributed monitoring and control systems. The system, an improvement of a VME-UDP/IP based system developed by our group for interferometric detectors of gravitational waves, is based on a dual-channel 18-bit low noise ADC and 16-bit DAC module at 1 MHz, managed by an ALTERA FPGA, that can be used standalone or mounted as mezzanine (also in parallel with other modules) on a motherboard. Both the modules and the motherboard can send/receive the configuration and the acquired/correction data for control through a standard EPP parallel port to an external PC, where the real-time computation is performed. Experimental tests have demonstrated that this architeture allows the implementation of distributed control systems, using a standard laptop PC for the real-time computation, with delay time $\Delta t < 30\,\mu s$ on a single channel, that is a sustained sampling frequency $f_c > 30\,kHz$. Each module is also equipped with a 20-bit slower ADC necessary for the acquisition of an external calibration signal. The system is now under extensive test in two different experiments, i.e. the control of a Michelson Interferometer to be used as Velocimeter for Seismic Waves in Geophysics and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators, a prototype for mirror control for Interferometric Detectors of Gravitational Waves.

Keywords: Remote Control Systems, Real-time Systems, Data Acquistion, Seismic Sensors

1. INTRODUCTION

Automatic control systems may require computing powers often quite difficult to be provided by embedded systems. In fact, in particular in distributed control system characterized by many inputs and outputs, the computing power necessary for control signal generation may be quite large, due to the need that all the operations of acquisition, control signal generation and signal distribution to the actuators to be geographycally distributed and synchronously performed at the chosen sampling frequency, f_c. To overcome the problem of the control computing power, an efficient and, nowadays, standard solution is that of using Digital Signal Processors (DSP), integrated in the acquisition and control system. This is what is currently done, for example, in the control system of the Interferometric Detector of Gravitational Waves Virgo.[2] Nonetheless, although efficient, this solution may be expensive and not versatile, so that may be not suitable for small experiments, remote sensors, embedded systems or, simply, for R&Ds. Some years ago we started to search and to analyze different solutions that could be more efficient for our purposes. Among the possible solutions, if the constraint on the sampling frequency of the control systems can be considered not stringent ($f_c < 100kHz$), then is is possible to use a standard communication link (e.g. Ethernet, Serial lines or Parallel ports) to link the acquisition and actuation units to a separate computing unit, like a Personal Computer or a PC farm. The great advantage of using a remote

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computing unit, is that the computing power becomes completely independent from the acquisition/actuation units, depending only on the characteristics and performances of the chosen computing unit. Therefore, the acquisition/actuation units can be remote low-power systems, provided with a suitable link and a transmission protocol on board.

The idea of linking the acquisition/actuation units with the computing unit through standard asynchronous protocols actually seems to conflict with the obvious requirement of control systems that the link among these units must be in principle synchronous. Actually, if the asynchronous data transfer is so fast that the sampling frequency of the control system is statistically guaranteed to be sustained, then the link can be considered as synchronous from the point of view of control theory. This system will be called in the following a Hybrid Acquisition and Control System. Keeping this idea in mind, we started to think to a building block of the system that could easily integrated with the standard COTS while retaining real-time and high sensitivity characteristics. The result is a board that integrates ADC, DAC, a default connection link and the possibility of using any other connection link as a plug-in. The development of this board started from the idea of a modular card to be assembled in up to six copies on a motherboard.[1] The motherboard hosts the default link, the main processor and a bus where the ADC/DAC modules can be connected. The ADC/DAC module has been designed, prototyped and tested on a NIOS development kit used as motherboard at the INFN in Napoli and in the Virgo Laboratory in Napoli using Ethernet, RS232 and Enhanced Parallel Port (EPP - IEEE1284) to connect to a PC. Then the communication logic has been embedded in the module's FPGA, and the module itself has been tested standalone in connection with a PC through a standard EPP. In this paper we discuss this solution and the performances of the system. In fact, the system is now under extensive test in two different experiments: the control of a Michelson Interferometer to be used as Velocimeter for Seismic Waves in Geophysics and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators, a prototype for mirror control for Interferometric Detectors of Gravitational Waves.[3]

2. PRELIMINARY STUDIES

The idea of controlling a system by means of a hybrid system has been tested with a VME-UDP/IP based system as explained in Acernese et al. (2006).[1] If we consider the Data Acquisition Time T_{DA}, the Data Transfer Time T_{DT} and the Data Processing Time T_{DP}, then the time necessary to generate the control signals from the acquired analog signals is:

$$T_{DM} = T_{DA} + 2T_{DT} + T_{DP} < 1/f_c \qquad (1)$$

where f_c is the loop *control* frequency, i.e. the maximum frequency that the system can control. A classical test application simply acquires a known signal (e.g. a sine wave) with a fixed sampling frequency f_s, sends along the link the ADC samples to the computing unit, and, as a first step sends them back through the link to the control unit where the data are converted into analog signal and observed with a scope against the input signal. With this configuration the term T_{DP} is essentially the time the computing unit takes to receive the data and send them back and the sum $2T_{DT} + T_{DP}$ is the Round Trip Time (RTT) of the chosen link technology. The first test with this VME-UDP/IP setup has shown that the control signal delay is approximately 2 samples at a maximum sampling frequency of $6.2\,kHz$.

3. THE INTEGRATED SYSTEM

3.1. Concept and implementation

To make the hybrid acquisition and control more useful for on-field applications, we are developing a board that integrates all the functionalities of the control unit. This board (see Figure 1) is based on the Cyclone® (or Stratix®) family of Altera CPUs and the NIOS II® development kit. The main component of this board is a daughterboard containing two independent channels. The daughterboard has two $\pm\,10\,V$ differential input and two differential $\pm\,10\,V$ outputs on a load of $1\,k\Omega$. Each channel contains a 18-bit ADC (AD7641), a dual 16 bit DAC (AD5545) whose section A is used as Programmable Gain Amplifier (PGA) and section B to set the offset, a 20-bit DAC (BurrBrown DAC1220) used for calibration and a 14 bit ADC to measure the internal temperature and allow an on-line correction. Each channel can be used either as a *fast* 16-bit DAC with a settling time of $0.5\,\mu s$ or as a 18-bit ADC with a maximum theoretical conversion rate of $2\,Msamples/s$. Alternatively the
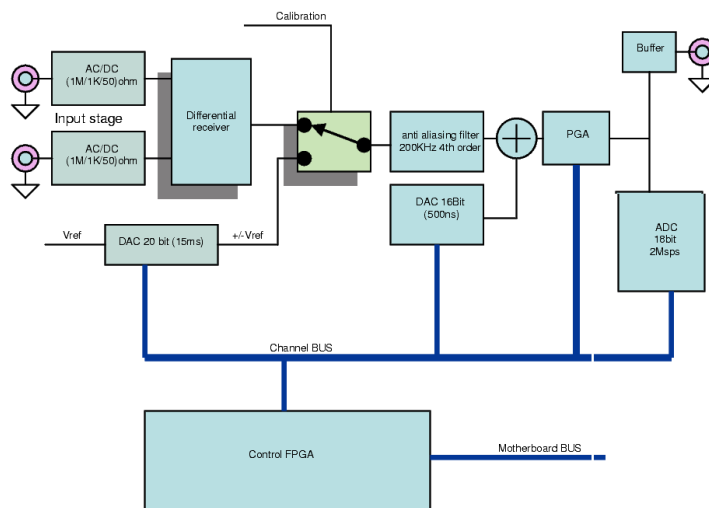
Figure 1. Input channel schematics

channel can be used as a 18-bit ADC and, at the same time, a 20-bit DAC with a settling time of $2\,ms$. The ADC trigger signal can be either internally generated on the daughterboard Programmable Logic Device (PLD) or taken from an external signal. An analogic 4th order anti-aliasing filter is placed both on the input and the output path. In Figure 2 the Prototype of the Module is shown in standalone configuration.
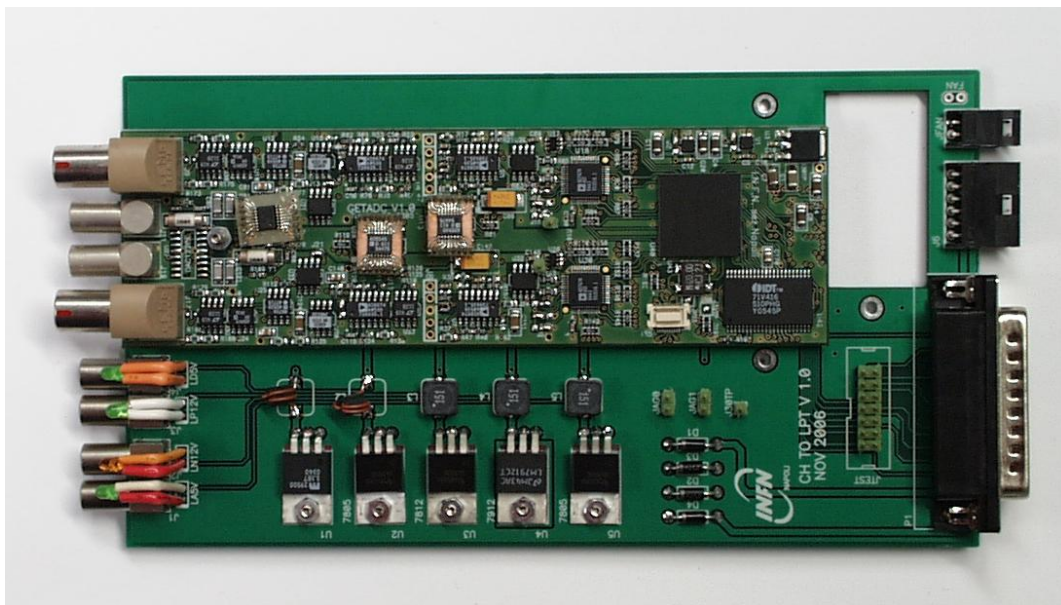

Figure 2. The Prototype of the Module in standalone configuration

3.2. Performance tests

The first prototype, implemented to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone® development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency. The NIOS kit was programmed in C language by means of the Altera Quartus II® development software. The PLD on board the module was not used at all.

With this prototype, we performed tests on the ADC performance, the different possible communication links and their speed. To test the ADC, we simply acquired a sine wave with a $1\,kHz$ frequency and $50\,mV$ or $120\,mV$ peak to peak amplitude. A simple program on the NIOS, allowed the acquistion in memory of 1 second of data and then transmit them to the PC through the RS232. We then evaluated the residuals of a fit with a sine function. The results are shown in Figure 3, and show a value of ± 6 ADC counts, both at $50\,mV$ and $120\,mV$, resulting from the convolution of both the ADC and the generator precision. Therefore, for a 18 bits and a $\pm 10\,V$ scale, this means a precision of $12 \times 20\,V/2^{18} \sim 9.2 \times 10^{-4}\,V$.
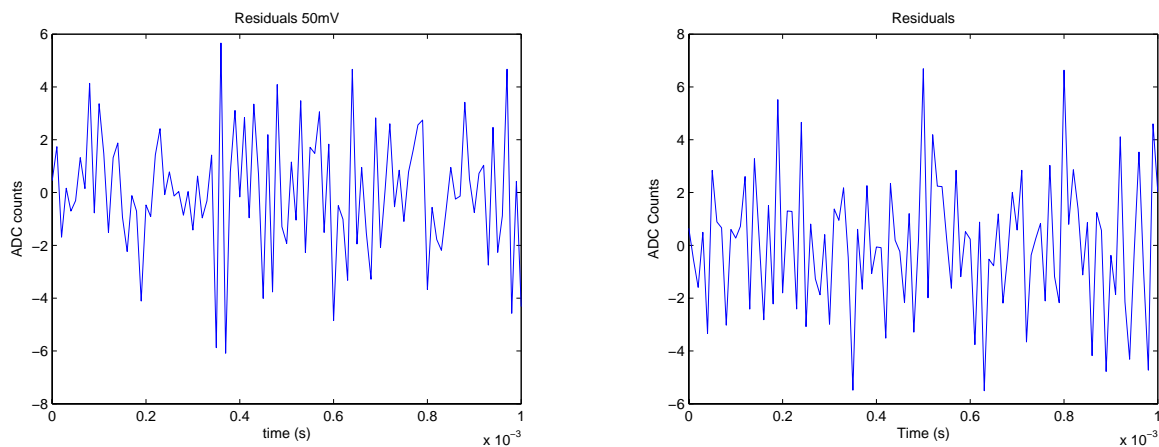

Figure 3. Difference between the ADC read value and the input sine wave for $50\,mV$ and $120\,mV$ amplitude. The input sine wave estimation is the result of a fit.

As far as the link tests are concerned, the fast Ethernet solution, as explained in the paper by F.Garufi et al.,[1] has resulted very slow. We then tested the complete signal round-trip by using a Linux laptop connected with a RS232 port as computing unit, obtaining a maximum allowable sampling frequency of 1.25 kHz (see Figure 4).

We, then, developed the idea to use the ADC-DAC module standalone, without the help of a motherboard, using a parallel port as communication link. The PLD on board the module has been programmed in VHDL in order to manage a protocol over an Enhanced Parallel Port (EPP), that allows to program and read the internal module registers from the remote PC. The C language program, used to program the NIOS development kit, has been transported on the PC and adapted to use this protocol. This solution allows to drive only one module per parallel port. With this setup we again tested the complete signal round-trip, obtaining a maximum allowed sampling frequency of $\sim 40kHz$. In Figure 5 a test with a $33\,kHz$ frequency is shown.

In this new 'standalone' architecture it is also considered the possibility of acquiring samples at the maximum speed allowed by the ADC, and decimate the samples at the external clock arrival. To this purpose a simple anti-aliasing digital filter must be implemented on the board, using the on-board SRAM.

3.3. Applications

Although this device has been designed to be used in fast control systems such as laser interferometry controls, the coexistence in the same board of ADCs, DACs and external link makes this object very promising for many applications. In fact, the system is now under extensive test in two different experiments, i.e. the control of a
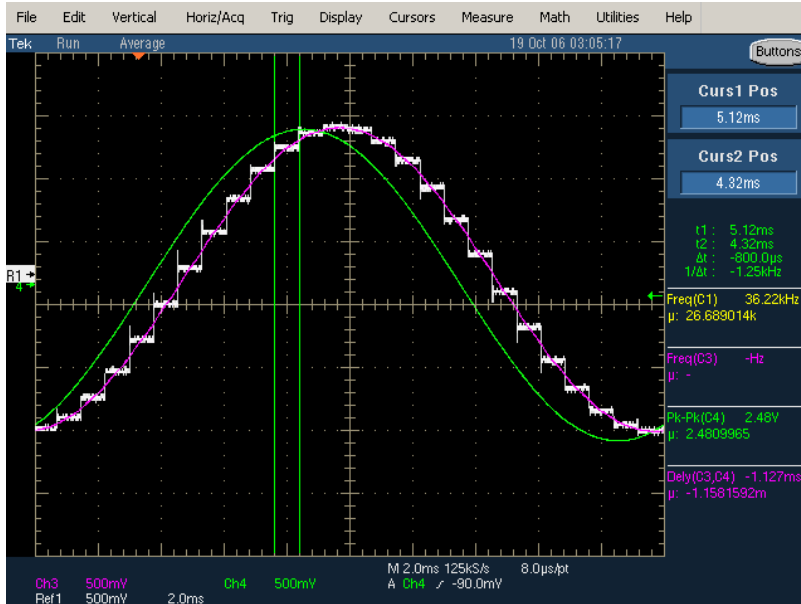
Figure 4. Serial RS232 line test. The continuous signal is the signal entering the ADC, the stepped one is the signal coming from the DAC. The sampling frequency is the step width and is determined by the link speed.
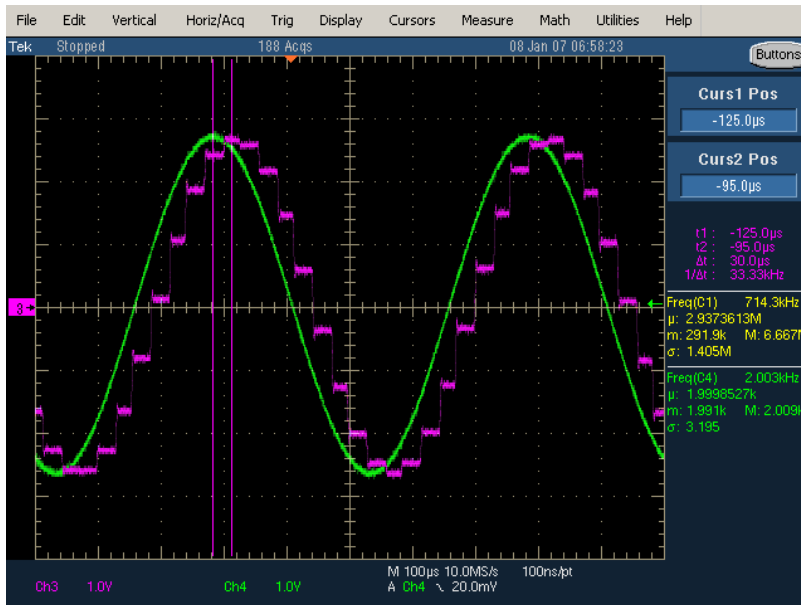

Figure 5. Parallel EPP line test. The continuous signal is the signal entering the ADC, the stepped one is the signal coming from the DAC. The sampling frequency is the step width.

Michelson Interferometer to be used as Velocimeter for Seismic Waves in Geophysics and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators, a prototype for mirror control for Interferometric Detectors of Gravitational Waves.[3] The first experimental results will be soon available.

4. CONCLUSIONS

We have designed and prototyped a hybrid acquisition and control system with an on-board communication link. This solution allows the collection of data from geographically distributed modiules into a central control station and the actuation/tuning on the basis of the collected data. The preliminary tests shown that the system developed can sustain a sampling frequency of $f_c > 30\,kHz$ with the standard protocol over an Enhanced Parallel Port (EPP). The system is now under extensive test in two different experiments: i.e. the control of a Michelson Interferometer to be used as Velocimeter for Seismic Waves in Geophysics and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators, a prototype for mirror control for Interferometric Detectors of Gravitational Waves.[3]

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