# Hybrid control and acquisition system for remote sensing systems for environmental monitoring

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## ABSTRACT

In this paper we describe the architecture and the performances of a hybrid acquisition system prototype we implemented in Napoli for remote sensing applications, which allow the fusion of multi-source data produced by environmental noise sources. In particular, we discuss how the system is able to integrate geographically distributed sensors for seismic, electromagnetic, acoustic, etc. noises, sampled at different frequencies, too. This system is an improvement of the environmental monitoring system developed by our group for interferometers for gravitational wave detection. In this paper we discuss the system, together with its characteristics and performances in connection with its application for the implementation of a geographically distributed monitoring system.

**Keywords:** Data acquisition, Remote Control

## 1. INTRODUCTION

In automatic control systems, often, the computing power needed to compute the necessary digital filters can make it difficult for an embedded system to sustain the control rate. To overcome this problem, the usual solution is the use of Digital Signal Processors (DSP), integrated in the acquisition and control system; this is what is currently done, for example, in the control system of the VIRGO experiment for Gravitational Waves search.[1] Nonetheless, this solution is economically and electrically expensive, and thus not suitable for small experiments, remote sensors or R&Ds. The alternative solution, thought for not too high control frequencies, is to use a standard acquisition and actuation system connected via a standard communication link (e.g. Ethernet) to a separate computing unit, as a Personal Computer or a PC farm that computes the filters and gives back the filtered data to the control system. In this way the acquisition/control subsystem can be also a remote low-power system, provided it has a suitable link and a transmission protocol on board. We call it a Hybrid acquisition and control system. Keeping this solution in mind, we started to think to a building block of the system that could easily integrate with the standard COTS while retaining real-time and high sensitivity characteristics. It is a board that integrates ADC, DAC, a default connection link - Ethernet - and the possibility to use any other connection link as a plug-in. The board has been designed to be modular: a motherboard hosts the default link, the main processor and a bus where the ADC/DAC modules can be connected. The ADC/DAC module has been designed and prototyped and is now in the phase of integration and characterization in the Napoli INFN and University laboratories. The motherboard is in advanced design phase, and has been partially prototyped to test the integration with the modules.

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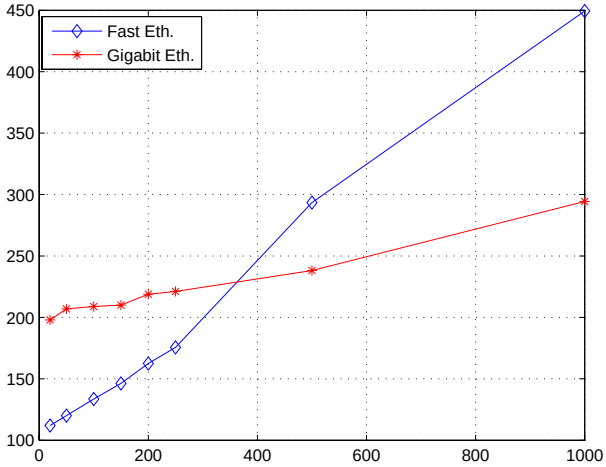


**Figure 1.** UDP Round trip times (RTT) in microseconds as a function of packet size in bytes for Fast Ethernet and Gigabit Ethernet, taking into account the context switch between processes

## 2. PRELIMINARY STUDIES

To test the idea, we built a hybrid acquisition and control system, based on standard VME real-time boards for the acquisition and control part and a PC for the computation of filters. The acquisition and control part was composed of a VMPC6a, a PowerPC VME board by Thales Computers, as the control unit, a 32 channels 16 bit ADC, the VGM/VGD5 by Pentland Systems and a 8 channels 16 bit DAC, the MPV955 by Pentland Systems. The control unit is equipped with a PMC slot to host an additional PCI (PMC form factor) communication board, and has an on-board 10/100 Ethernet. The communication between the control unit and the ADC and DAC is through the VME bus, and the control unit runs the LynxOS 4.0 hard real-time operating system by LynuxWorks. On this system we tested a simple application to check the minimum loop time allowed by the link speed. If we consider the Data Acquisition Time $T_{DA}$, the Data Transfer Time $T_{DT}$ and the Data processing time $T_{DP}$, then the time necessary to generate the control signals from the acquired analog signals is:

$$T_{DM} = T_{DA} + 2T_{DT} + T_{DP} < 1/f_c \tag{1}$$

where $f_c$ is the loop "control" frequency, i.e. the maximum frequency that the system can control. Our test application simply acquires a known signal (e.g. a sine wave) with a fixed sampling frequency $f_s$, sends along the link all the 32 ADC samples to the computing unit, and, as a first step sends them back to the control unit along the link where the data are converted into analog signal and observed with a scope against the input signal. With this configuration the term $T_{DP}$ is essentially the time the network stack of the computing unit takes to receive the data and send them back in a new packet and the sum $2T_{DT} + T_{DP}$ is the Round Trip Time (RTT) of the chosen link technology plus the data transfer times along the VME bus.

We preliminarily evaluated the RTT for both Fast Ethernet and Gigabit Ethernet link, with UDP protocol, as a function of the packet size with a simple test program and we found that, for the small packet sizes involved with our application, Fast Ethernet is more efficient (or at least equivalent see Fig.1) because it has a lower latency if we use two processes to transmit and receive. We thus selected the Fast Ethernet interface on-board the VMPC6a to transmit and receive data and developed an acquisition and control program using a single process to acquire data from the ADC transmit them on the link, receive back from the computing unit via UDP/IP. The alternative solution of using a raw protocol to improve the link speed has been discarded because the time to build the packet in user mode is comparable to the time the kernel uses to build an UDP packet, and the overhead is minimal. The first test with this setup has been the acquisition of a sine wave and its reconstruction

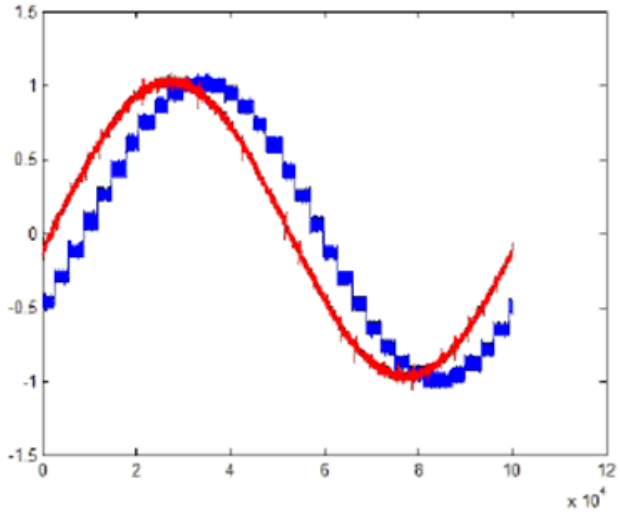


**Figure 2.** Time delay introduced by the control system without any filtering; in red the input signal,in blue the exit from DAC. The signal has been acquired with a 6.2 kHz clock, which is the maximum allowed by our ADC software driver. The x axis unit is the scope sample number.

with the DAC after passing it from the computing unit. As can be seen from Fig. 2, the control signal delay is approximately 2 samples at a sampling frequency of 6.2 kHz. This sampling frequency is determined by the packet round trip and by the characteristics of the software driver we wrote to drive the VME ADC. With a RTT of the order of 125 $\mu s$, the maximum allowed sampling time would be 8 kHz; since the ADC driver does not handle the internal ADC FIFO we cannot allow data to pile up in the ADC to avoid the system to block, thus the maximum allowed frequency is lower than 8 kHz and has been experimentally found to be 6.2 kHz. We found that, for our usual application,the filtering activity on the computing unit, consisting in calculating FIR filters, accounts for a few more microseconds apart the filter time lag and does not affect significantly the system performances. With this setup, we could control a suspended Michelson laser interferometer acting on three degrees of freedom of the suspended mirror, with a sampling and control frequency up to 5 kHz.

## 3. THE INTEGRATED SYSTEM

### 3.1. Concept and implementation

To make the hybrid acquisition and control more useful for on-field applications, we are developing a board that integrates all the functionalities of the control unit. This board (see Figure 3) is based on the Cyclone© (or Stratix© family of Altera CPUs and the NIOS II© development kit. The main component of this board is a daughterboard containing two independent channels. The daughterboard has two $\pm 10\ V$ differential input and two differential $\pm 10\ V$ outputs on a load of $1k\Omega$.
Each channel contains a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545) whose section A is used as Programmable Gain Amplifier (PGA) and section B to set the offset, a 20 bit DAC (BurrBrown DAC1220) used for calibration and a 14 bit ADC to measure the internal temperature and allow an on-line correction.
Each channel can be used either as a "fast" 16 bit DAC with a settling time of 0.5 $\mu s$ or as a 18 bit ADC with a maximum theoretical conversion rate of 2 $Msamples/s$. Alternatively the channel can be used as a 18 bit ADC and, at the same time, a 20 bit DAC with a settling time of 2 $ms$.
The ADC trigger signal can be either internally generated on the daughterboard Programmable Logic Device (PLD) or taken from an external signal.

The logic to manage ADC and DACs and the interfacing with the motherboard is performed by a Cyclone PLD, hosted on each channel. Up to 8 channels will be hosted on a motherboard which will provide the fast Ethernet interface and a PMC slot to host eventual different communication links, and will manage the packing,

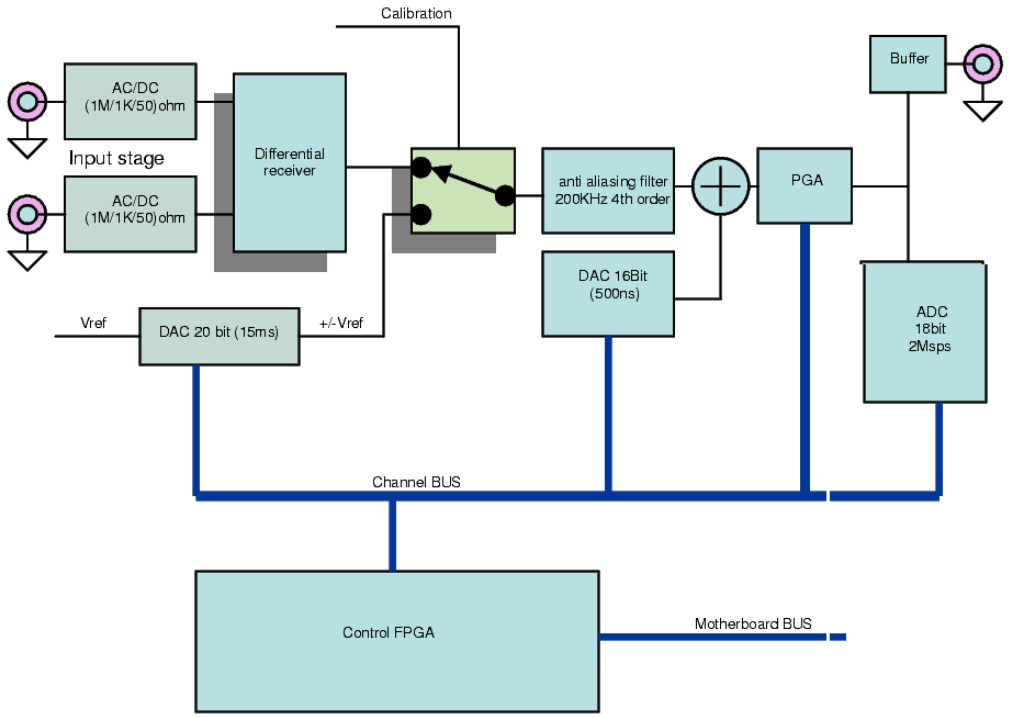


**Figure 3.** Input channel schematics

transmission reception and dispatching of the data. A complete prototype of the daughterboard has been built and is under test in our laboratory with the help of a NIOS II development kit used as main board and is shown in Figure 4.

The software to manage the channel hardware has been developed with the Quartus II© development software and software to interface the channel with the development kit and manage the Ethernet communication is being developed using the Nios II IDE and the MicroC/OS-II real time operating system. With this Hardware/Software combination we could test the internal clock generation, and the digital to analog conversion, both on the 16 and the 20 bit DACs.
At each clock tick, the converted value from each ADC on the motherboard is written in sequence on a FIFO memory and the sequence is preceded by a timestamp so that each piece of data is recognizable in terms of time and source, only by knowing the number of ADCs enabled on the board.
The first tests on the UDP transmission/reception with the Nios II Stratix II development kit show a slower link speed with respect to the VME test prototype. The same network test performed in the preliminary study with a VMPC6a has been repeated with the development kit, giving RTT=1.7 ms with a packet size of 200 bytes, i.e. 7 times slower than the value measured with the VME system. This high RTT is partly due to the poor performance of the Ethernet interface on board the kit, which is reported to give 5.16 Mbps in transmission and 3.44 Mbps in reception.[2] This would give a total of 0.8 ms to transmit and receive 200 bytes, which is still about one half than the measured value. The time between two packets, anyway, is 1.72 $ms$ which give a frequency $f_c = 581$ Hz to close the loop. This is the maximum control frequency with this hardware/software combination.

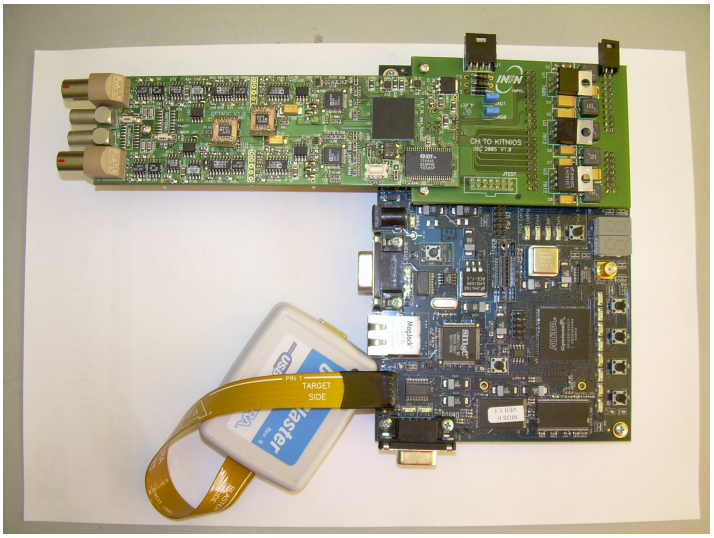


**Figure 4.** The full prototype of the daughterboard, mounted on the Nios II development kit.

### 3.2. Possible applications

Although this device is thought to be used in fast control systems such as laser interferometry controls, the coexistence in the same board of ADCs, DACs and Ethernet link makes this object very promising for use in remote sensing. It is a low consuming device that can be powered with a car battery and can be a building block for a remote sensing network as e.g. a seismic, spontaneous potential, magnetometric measurement network on a volcanic cone, eventually in conjunction with a wireless point of access where an ethernet link is not available. The ADC/DAC combination allows also the actuation or the tuning of other instrumentation on-board the remote sensing station on the basis of the collected data analysed by the central control system.
The high resolution of the on-board ADCs and DACs suggests a possible application in the precision measurement of displacements e.g. with optical levering or electrostatic sensing techniques. The presence of several channels on a single board and the transmission link makes it possible to build e.g. fine grained displacement/velocity fields.

## 4. CONCLUSIONS

We have designed and prototyped a hybrid acquisition and control system with an on-board Ethernet link. This solution allows the collection of data from geographically distributed sensors into a central control station and the eventual actuation/tuning on the basis of the collected data. The preliminary tests indicates that the networked control can work at least at 6kHz with standard technology, and that the integrated prototype can acquire, send, receive and reconvert data.

## REFERENCES

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