Hybrid control and data acquisition system for geographically distributed sensors for environmental monitoring

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ABSTRACT

In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype for environmental monitoring and geophysics. The system, an improvement of a VME-UDP/IP based system we developed for interferometric detectors of gravitational waves, is based on a dual-channel 18-bit low noise ADC, a 16-bit DAC module at $1\,MHz$, and a 20-bit slower ADC necessary for the acquisition of an external calibration signal. The module can be configured as stand-alone or mounted on a motherboard as mezzanine in parallel with other modules. Both the modules and the motherboard can send/receive the configuration and the acquired/correction data for control through a standard EPP parallel port to a standard PC, where the real-time computation is performed. Experimental tests have demonstrated that the distributed control systems implemented with this architecture exihibit a delay time of less than $25\,\mu s$ on a single channel, that is a sustained sampling frequency of more than $40\,kHz$. The system is now under extensive test in two different experiments: the remote control and data acquisition of a set of seismometers, velocimeters and accelerometers to simulate a geophysics networks of sensors and the remote control of the end mirrors of a suspended Michelson interferometer through electrostatic actuators for interferometric detectors of gravitational waves.

Keywords: Remote Control System, Real-time Systems, Data acquisition, Environment Monitoring.

1. INTRODUCTION

The architecture of a geographically distributed data acquisition systems for environmental monitoring is classically based on local acquisition units, directly interfaced to the sensors, and on a central supervisor unit, that collects and store the data from the local units, synchronize the processes, and monitor and supervise the whole acquisition process. Many efficient technical solutions are available, based on different communication protocols, local data synchronisation and data storage. Nevertheless the design and implementation of a geographically distributed data acquisition system (e.g. a geographically distributed environmental monitoring system) becomes quite difficult when data acquisition is dependent on the centralized automatic control of the local sensors and systems. In fact, all the operations realtive to the control must be perfectly synchronized at the control frequency, f_c. The synchronization of data acquisition process is less stringent, being it necessary only the synchronization of local data acquisiton (e.g. with local GPS) at f_s, while the data transfer to the central unit and to the archiving system can be performed in blocks of data (frames), whose reconstruction and processing can be performed also off-line. Therefore, the data acquisition frequency, f_s may differ and be higher than the control frequency, f_c.

On the other hand, the requirement of synchronous communications at f_c among the local units and the central one largely reduces the number of suitable communication protocols and architectures. Today many efficient and reliable solutions exists, like for example the one based on Digital Signal Processors (DSP) based

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on VME bus and operating systems like LynxOS. We have adopted this technique for the control system of the Interferometric Detector of Gravitational Waves Virgo[1,].[2] Nonetheless, although very efficient, these solutions may result very expensive, difficult to handle, sometimes very critical and not versatile for the control of remote sensors and system, both for applied R&D and industrial apparata. Therefore, some years ago we began to test and develop possibile architectures capable to satisfy the general requirements of data acquisition and control of geographically distributed systems and sensors, both for control of interferometric prototypes for gravitational wave detection and for environmental monitoring and geophysics. We have developed many prototypes and performed a large number of tests, using standard communication protocols for communication. These tests have demonstrated that configurations using standard communication protocols (e.g. Ethernet, serial or parallel lines) to link the local units to the central one (a Personal Computer or a farm configured as a global controller) may be very useful and convenient if the constraints on the sustained sampling frequency of the control systems are not stringent ($f_c < 100\,kHz$)[3,4,5,].[6]

Actually, the idea of linking the acquisition/actuation units with the computing unit through standard asynchronous protocols actually seems to conflict with the obvious requirement of control systems, i.e. a synchronous link among the units. But this constraint can be overcome if the asynchronous data transfer is so fast that the sampling frequency of the control system is statistically guaranteed, so that the link can be considered synchronous from the point of view of control theory. This solutions does not prevent the use of the standard oversampling techniques for input digital noise reduction, but have the great advantage that the central unit can be defined and chosen in a completely independent way from the acquisition/actuation unit. Therefore, for example, the acquisition/actuation unit can be also a remote low-power system, equipped with a suitable link and a transmission protocol on board for connection with the computing unit. In the following, this system will be called *Hybrid Acquisition and Control System*. Keeping this idea in mind, we have designed and implemented a basic module with two ADCs and two DACs on board, with real-time and high-sensitivity characteristics, that could be easily integrated with the standard COTS. We included also a default connection link, keeping anyway the possibility of using any other connection link as a plug-in. The global architecture of this board started from the need of developing a modular card to be assembled in up to six copies on a single motherboard[3,4,5,].[6] The motherboard hosts the default link, the main processor and a bus where the ADC/DAC modules can be connected. The ADC/DAC module has been designed, prototyped and tested on a NIOS development kit used as motherboard at the INFN in Napoli. Several communication protocols have been tested in this phase: Ethernet, RS232 and Enhanced Parallel Port (EPP - IEEE1284). Then the communication logic has been embedded in the module's FPGA, and the module itself has been tested standalone in connection with a PC through a standard EPP.

In this paper we discuss the configuration and the performances of the system of the *Hybrid Acquisition and Control System* applied to the distributed control and data acquistion of a Michelson Interferometer protoype with suspended mirrors controlled with electrostatic actuators, that is part of a R&D for the development of a second generation of interferometric detectors of gravitational waves.

2. THE MODEL

The idea of controlling a system by means of a hybrid system has been tested with a VME-UDP/IP based system[3,4,5,].[6] If we define the Data Acquisition Time (ADC and DAC data conversion times), T_{DC}, the Data Transfer Time, T_{DT} and the Data Processing Time, T_{DP}, then the time necessary to generate the control signals from the acquired analog signals, T_{DM}, is:

$$T_{DM} = T_{DC} + 2 \cdot T_{DT} + T_{DP} < 1/f_c \tag{1}$$

where f_c is the loop *control* frequency, which defines the maximum control band of the system. These parameters can be easily measured through simple application test: a known signal (e.g. a sine wave) with a fixed sampling frequency, f_s, is digitized by the ADC and sent through the link to the computing unit; the latter simply send it back to the DAC, that converts it again in an analogic signal. The input signal and the output signal are observed with an oscilloscope. Being in this test $T_{DP} = 0\,s$, hence the measured quantity is the Round Trip Time, $RTT = T_{DC} + 2 \cdot T_{DT}$, that is the time the whole system takes to convert, transfer through the chosen link technology and convert back the data. For what concerns T_{DP}, it is only possible to underline that it depends

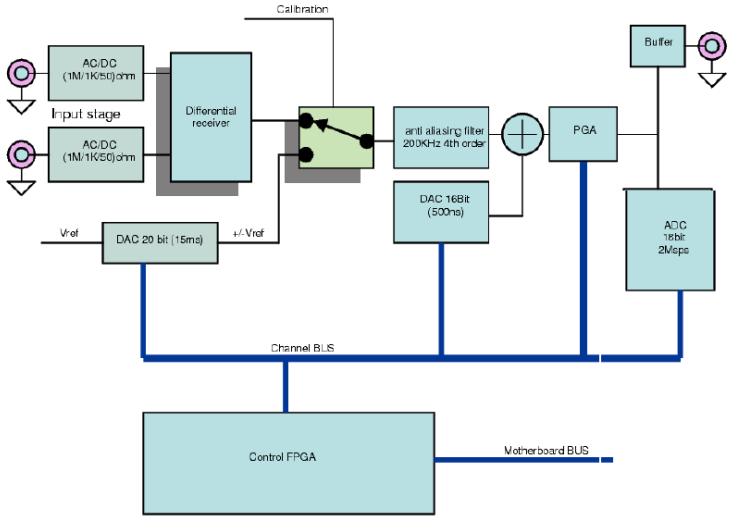

Figure 1. Input channel schematics.

on the available computing power and on the complexity of the real-time computation. Nonetheless, taking into account the very high computing power of the state-of-the-art computing units, it can be considered negligigle with respect to T_{DC} and T_{DT} in most cases. The first tests performed with a VME-UDP/IP setup have shown that the control signal delay was approximately 2 samples at a maximum sampling frequency of $6.2\,kHz$.[3] Since this result was quite far from our goals, we decided to test different protocols. We describe the architecture and the results in the following sections.

3. THE INTEGRATED SYSTEM

3.1 Concept and implementation

In order to make the hybrid acquisition and control more useful for on-field applications, we have developed a board that integrates all the functionalities of the control unit. This board (see Figure 1) is based on the Cyclone® (or Stratix®) family of Altera CPUs and the NIOS II® development kit. The main component of this board is a daughterboard containing two independent channels. The daughterboard has two $\pm 10\ V$ differential input and two differential $\pm 10\ V$ outputs on a load of $1\,k\Omega$. Each channel contains a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545) whose section A is used as Programmable Gain Amplifier (PGA) and section B to set the offset, a 20 bit DAC (Burr-Brown DAC1220) used for calibration and a 14 bit ADC to measure the internal temperature and allow an on-line correction. Each channel can be used either as a *fast* 16 bit DAC with a settling time of $0.5\,\mu s$ or as a 18 bit ADC with a maximum theoretical conversion rate of $2\,Msamples/s$ (for the first prototype a $800\,kHz$ ADC – AD7674 – is used). Alternatively the channel can be used as a 18 bit ADC and, at the same time, a 20 bit DAC with a settling time of $2\,ms$. The ADC trigger signal can be either internally generated on the daughterboard Programmable Logic Device (PLD) or taken from an external signal. An analogic 4^{th} order anti-aliasing filter is placed both on the input and the output path. In Figure 2 the daughter board is shown in the standalone configuration, while in Figure 3 the complete module is shown.

The advantage of this board compared to other similar systems available on the market, is the possibility to have a control band that can span continuously from the mHz to the tens of kHz, without the need of large oversampling. Other systems, based on $\Sigma - \Delta$ ADCs, are faster and more efficient on the high frequency range, but fail with slowly varying ($< 100\,Hz$) signals.

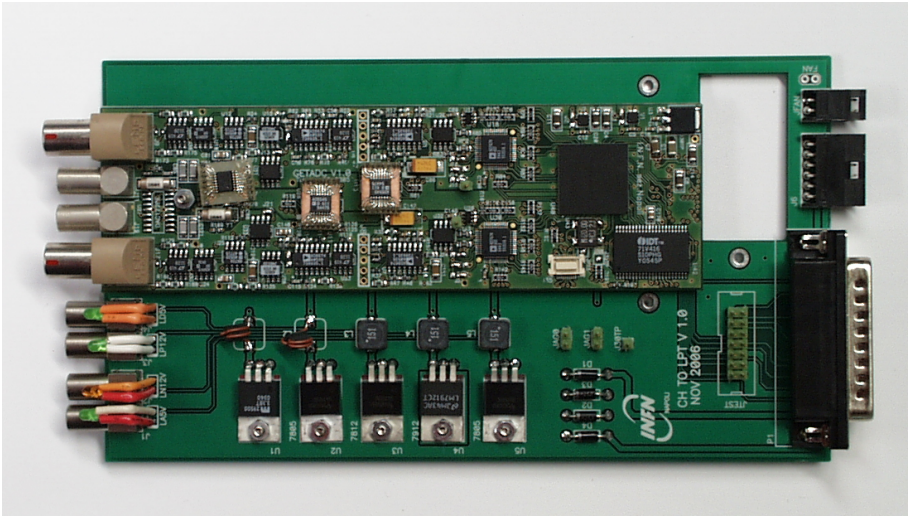

Figure 2. Daughter Board in standalone configuration. The hole in the power distribution base is to host the fan.

Figure 3. The Module in standalone configuration.

3.2 Performance Tests

The first prototype, realized to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency. The NIOS kit was programmed in C language by means of the Altera© Quartus II® development software. The PLD on board the module was not used at all.

With this prototype, we performed tests on the ADC performance and on different communication links. We evaluated the accuracy of the ADC by acquiring a sine wave and evaluating the residual with respect to the theoretical value. The results are shown in figure 4. A value of ± 6 ADC counts, both at $50\,mV$ and $120\,mV$, results from the convolution of both the ADC and the generator precisions. Assuming 18 bits over a $\pm 10\,V$ scale, this means a precision of $12 \times 20\,V/2^{18} \sim 9.2 \times 10^{-4}\,V$, although it should be a function of the sampling frequency.

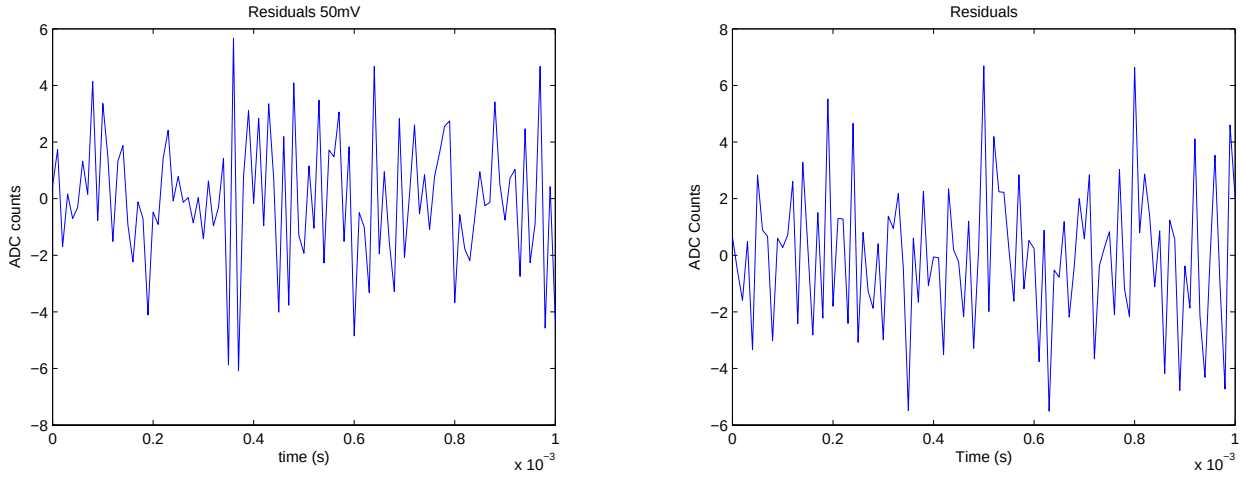

Figure 4. Difference between the ADC read value and the input sine wave for $50\,mV$ and $120\,mV$ amplitude. The input sine wave estimation is the result of a fit.

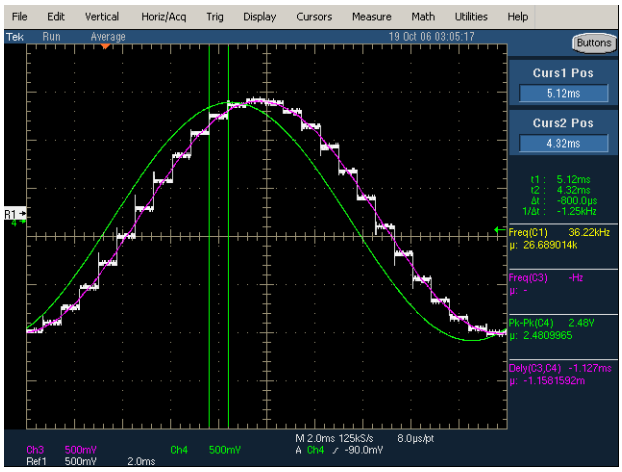

Figure 5. Serial RS232 line test. The continuous line is the signal entering the ADC, the stepped the signal coming from the DAC. The continuous curve just below the DAC signal is an average over 1 second of the DAC signal. The sampling frequency is the step width and is determined by the link speed.

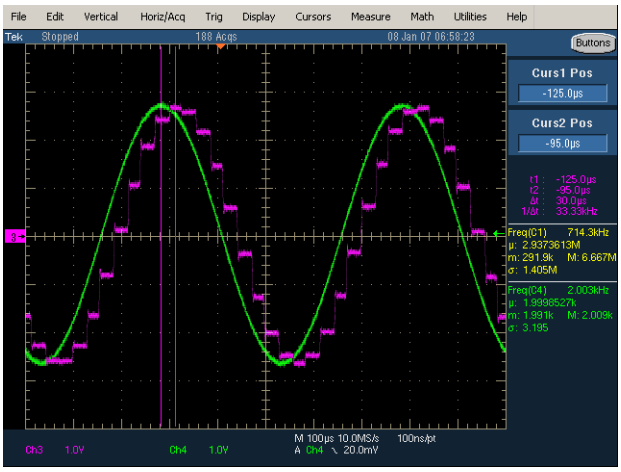

Figure 6. Parallel EPP line test. The continuous line is the signal entering the ADC, the stepped one the signal coming from the DAC. The sampling frequency is the step width.

As far as the link tests are concerned, the fast Ethernet solution produced very unsatisfactory results.[3] We then tested the complete signal round-trip by using a Linux laptop connected through a RS232 port as computing unit, obtaining a maximum sampling frequency of 1.25 kHz (see Figure 5).

We, then, decided to use the ADC-DAC module standalone, without the help of a motherboard, and to use a parallel port as communication link. The PLD on board the module has been programmed in VHDL in order to manage a protocol over an Enhanced Parallel Port (EPP), that allows programming and reading the internal module registers from the remote PC. This solution allows to driving only one module per parallel port. With this setup we again tested the complete signal round-trip, obtaining a maximum sustained sampling frequency of $\sim 40\,kHz$, although frequencies up to $80\,kHz$ could be reached if the time tag information is not enabled nor transmitted with data. In Figure 6 a test with a $33\,kHz$ frequency is shown.

This new *standalone* architecture gives also the possibility of acquiring samples at the maximum speed allowed by the ADC and of decimating the samples synchronously to an external trigger. To this purpose we developed

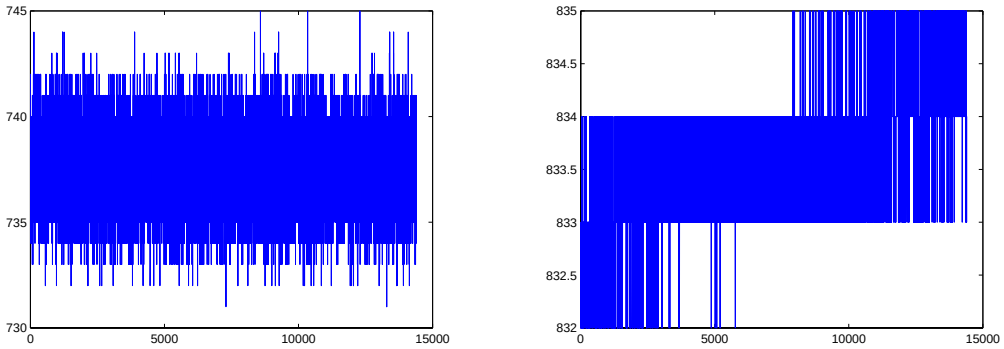

Figure 7. Internal noise acquired at $20\,kHz$ raw and filtered with the Moving Average. The horizontal axis is the sample number, the vertical axis is ADC counts.

on the board a digital moving average (MA) filter whose output is the average of the samples acquired between two trigger pulses, thus, for a trigger frequency of $10\,kHz$ and an ADC clock speed of $800\,kHz$, the acquired samples are the result of averaging $800/10 = 80$ ADC samples. In this way the same VHDL filter implementation can be used with any trigger frequency allowed by the communication link, while a more complicated filter would have required different numeric parameters for different frequencies.

To characterize the electronic and acquisition noises of the ADC, we acquired some seconds of data with the input closed on a $50\,\Omega$ termination, with and without the MA filter at different acquisition frequencies. Without the MA, we noticed a 10 LSB wide noise, while with the MA the *internal* noise is reduced to 2–3 LSB over the observed period at frequencies of 10 and $20\,kHz$, as can be seen in Figure 7. In the same figure, it is possible to see a trend in the MA data, that can be interpreted as a temperature effect, as will be explained later in the paper.

A 14 bit ADC is available to read an on board temperature sensor. The temperature information can be acquired without the need of a trigger pulse. In this way it is possible to correct the 18 bit ADC data taking into account the temperature drifts, by periodically acquiring the temperature information.

To test the effects of the temperature on the board we acquired the *terminated* input channel at different temperatures, using a moving average with a sampling frequency of $200\,Hz$. We noticed that the ADC counts are not a linear function of the temperature change, although it can be considered linear in intervals of about $5°C$. The fits show that the temperature coefficient takes values in the interval from ~ 4.5 to ~ 6.5 $counts/°C$ in the range $40 - 55°C$. In Figure 8, an example of the temperature measurements is shown.

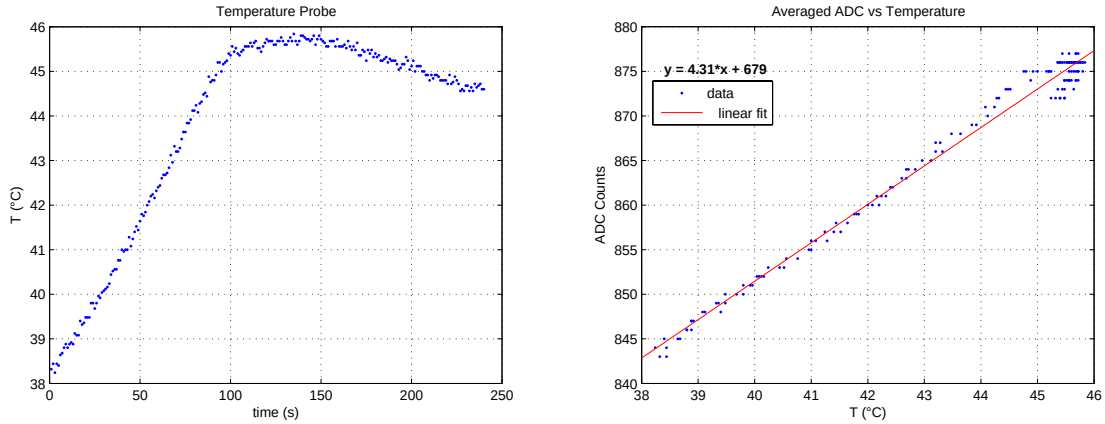

Figure 8. Temperature vs time as measured by the on-board temperature probe and averaged ADC counts as a function of the temperature.

Being these results very encouraging we have implemented a new prototype board with a $2\,MHz$ ADC with the same architecture described here. The first tests on this prototype show that the ADC is more noisy than the $800\,kHz$ model. Although this is expected from the product data sheets, giving a SNR of *101 dB* for the *800 kHz* and *96 dB* for the *2 MHz*, the larger number of averages per sample allowed by the higher ADC clock speed is not enough to compensate the difference. All the other parameters seem to be unchanged.

The choice of parallel port as communication link has been dictated by the availability of the hardware on most of present day personal computers. To increase the bandwidth of the control system we are now studying other possible solutions based on optical fiber interfaces, like e.g. firewire, infiniband, etc.

3.3 Applications

The system was extensively tested in the control of the end mirror of a suspended Michelson interferometer through electrostatic actuators. This is a prototype for mirror control for interferometric gravitational waves detectors. The optical set up is shown in Figure 9.

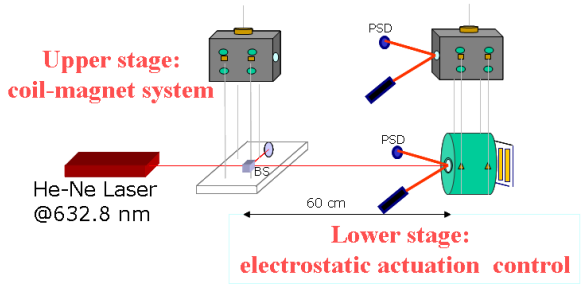

Figure 9. Suspended Michelson interferometer.

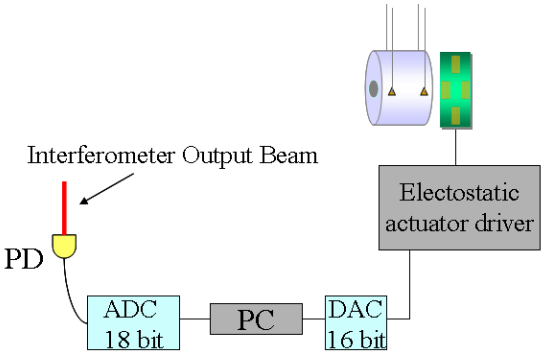

Figure 10. Lower stage control system architecture.

The first arm optics consists in a first interferometer mirror IM1 and two mirrors MA and MB. It is mounted on the lower stage of a double pendulum suspension. The position of its upper stage is controlled in both rotational and longitudinal degrees of freedom using coils-magnet system. The second mirror IM2 is suspended of a similar double pendular suspension. The upper stage is controlled in all degrees of freedom by means of coil-magnet actuator. For both upper stages the digital control is achieved by using a standard VME ADC-CPU-DAC architecture.

In the lower stage (Figure 10) we use the electrostatic actuator to control the mirror longitudinal movement. The digital control is achieved by using the 18 bit ADC-DAC described above and the lock is easily achieved.

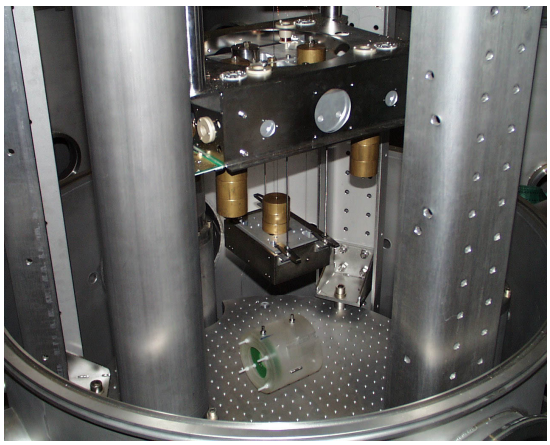

Figure 11. The mechanical suspension of the interferometric prototype.

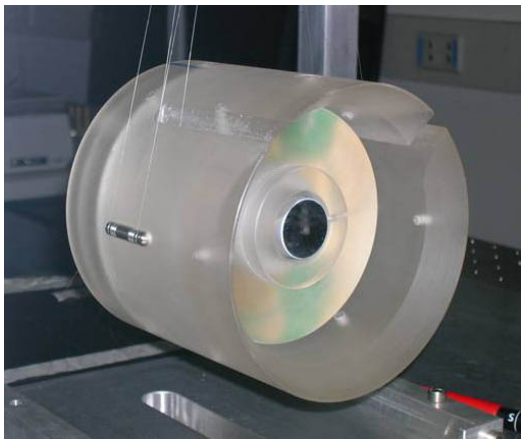

Figure 12. The lower stage of the suspensions with electrostatic actuators.

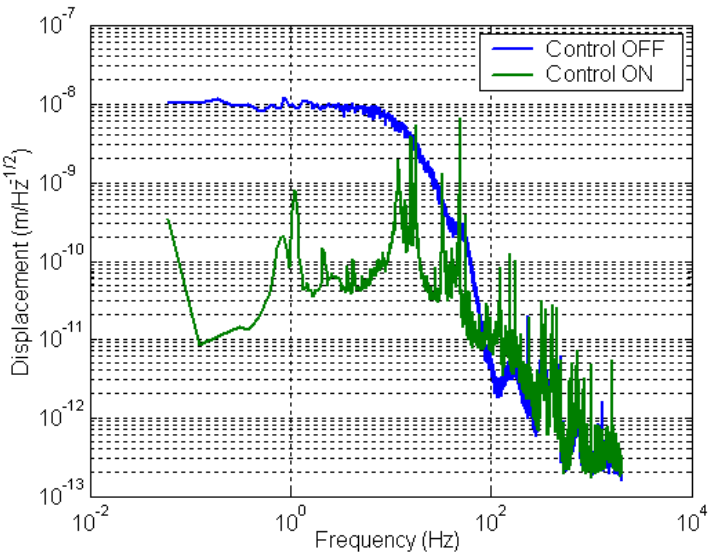

Figure 13. Preliminary results of the suspension lower stage control with electrostatic actuators.

In Figure 11 and Figure 12 the mechanical suspension of the interferometer prototypeand the lower stage of the suspension with electrostatic actuators, respectively. Preliminary results are shown in Figure 13.

To control different channels of the interferometer with a single board, a multiplexing/demultiplexing scheme has been proposed and is in a design study phase. The different channels can be acquired in sequence by means of a *fast* multiplexer, and the control signal can be obtained by demultiplexing the output DAC signal with a delay of one trigger tick with respect to the input. Finally this board is being tested used in standalone mode at the University of Salerno to monitor the output of a monolithic accelerometer with interferometric read-out. This is one of the preliminary tests necessary for the implementation of a geographically distributed environmental and geophysical network. The results of this test will be available soon.

4. CONCLUSIONS

We have designed and prototyped a hybrid acquisition and control system with an on-board communication link. This solution allows the collection of data into a control station and the actuation/tuning on the basis of the collected data. The preliminary tests have shown that the developed system can sustain a sampling frequency ranging from the mHz region to $f_c > 40\,kHz$ with a standard protocol over an Enhanced Parallel Port (EPP) and can enhance its precision by using an oversampling/averaging filter. The system is now under extensive test in two different experiments: i.e. the read-out and control of monolithic accelerometer with interferometric read-out at the University of Salerno and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators at the Univerisity of Napoli.

REFERENCES

1. F. Acernese et al., *Class. and Quantum Grav.*, **23**, S63 (2006).
2. F. Acernese et al. *Journal of Physics: Conference Series*, **32**, 35 (2006).
3. F. Garufi, F. Acernese, A. Boiano, R. De Rosa, R. Romano, F. Barone *Hybrid control and acquisition system for remote sensing systems for environmental monitoring*, Proc. of SPIE *Remote Sensing for Environmental Monitoring, GIS Applications, and Geology VI*, Stockholm, Sweden, September 11-16, SPIE Vol.6366, 636616 (2006).
4. F. Garufi, F. Acernese, A. Boiano, R. De Rosa, R.Romano, F.Barone *Hybrid control and acquisition system for distributed sensors for environmental monitoring*, in Sensor Systems and Networks: Phenomena, Technology, and Application for NDE and Health Monitoring 2007, edited by Kara J. Peters, Proc. of SPIE *Smart*

Structures and Materials & Nondestructive Evaluation and Health Monitoring 2007, San Diego (USA), SPIE Vol.6530, 65301M1-6 (2007).

5. F. Garufi, F. Acernese, A. Boiano, R. De Rosa, R. Romano, F. Barone *A hybrid modular control and acquisition system*, in Proc. of IEEE NPSS 15^th Real Time Conference, Fermilab, Batavia, Illinois (USA), April 29 - May 4 2007 (in press).
6. F. Garufi, F. Acernese, A. Boiano, R. De Rosa, R.Romano, F.Barone *A hybrid modular control and acquisition system*, *IEEE Trans. on Nucl. Sci.* (submitted).
7. F.Acernese, et al. *A Michelson interferometer for seismic wave measurement: theoretical analysis and system performances*, Proc. of SPIE *Remote Sensing for Environmental Monitoring, GIS Applications, and Geology VI*, Stockholm, Sweden, September 11-16, SPIE Vol.6366, 63660I-1-11 (2006).