A hybrid modular control and acquisition system

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***Abstract*—In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype we developed in Napoli for the implementation of geographycally distributed monitoring and control systems. The system, an improvement of a VME-UDP/IP based system developed by our group within the framework of R&D for interferometric detectors of gravitational wave, is based on a dual-channel 18-bit low noise ADC and 16-bit DAC module at 800 kHz, managed by an ALTERA FPGA. The module can be used standalone or mounted as mezzanine on a motherboard, in parallel with other modules, too. Both the modules and the motherboard can send/receive through a standard EPP parallel port the configuration and the acquired/correction signal for control to/from an external PC, where the real-time computation is performed. Experimental tests have demonstrated that this architeture allows the implementation of distributed control systems with delay time $\Delta t < 30\,\mu s$ on a single channel, that is a sustained sampling frequency $f_c > 30\,kHz$, using a standard laptop PC for the real-time computation. Each module is also equipped with a 20-bit slow ADC necessary for the acquisition of an external calibration signal. The system is now going to be extensively tested in two different R&D experiments, i.e. read-out and control of a monolithic accelerometer with interferometric read-out and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators, a prototype for mirror control for Interferometric Detectors of Gravitational Waves.**

***Index Terms*—Real-time digital control, Data acquistion.**

I. Introduction

Automatic control systems may require computing powers often quite difficult to be provided by embedded systems. In fact, distributed control systems are often characterized by many inputs and outputs, so that the necessary computing power for control signal generation may be quite high and it can be difficult to sustain the chosen sampling frequency, f_c. To overcome the problem of the control computing power, an efficient and, nowadays, standard solution is that of using Digital Signal Processors (DSP) integrated in the acquisition and control system. This is what is currently done, for example, in the control system of the Interferometric Detector of Gravitational Waves Virgo [1]. Nonetheless, although very efficient, this solution may be expensive and not versatile for small experiments, remote sensors, embedded systems or, simply, for R&D experiments. Some years ago we started to search and to analyze different configurations that could be more efficient for our purposes. We demonstrated that it is possible to use standard communication protocols (e.g. Ethernet, Serial lines or Parallel ports) to link the acquisition and actuation units to an independent computing unit, like a Personal Computer or a PC farm, if the constraint on the sustained sampling frequency of the control systems are not stringent ($f_c < 100\,kHz$) [2]. Of course, this configuration still allows the use of the standard oversampling techniques for input digital noise reduction, but its great advantage is that the computing power unit can be defined and chosen in a completely independent way from the acquisition/actuation unit. Therefore, for example, the acquisition/actuation unit can be also a remote low-power system, equipped with a suitable link and a transmission protocol on board for connection with the computing unit.

The idea of linking the acquisition/actuation units with the computing unit through standard asynchronous protocols actually seems to conflict with the obvious requirement of control systems, i.e. a synchronous link among the units. Actually, this constraint can be overcome if the asynchronous data transfer is so fast that the sampling frequency of the control system is statistically guaranteed, so that the link can be considered synchronous from the point of view of control theory. In the following, this system will be called *Hybrid Acquisition and Control System*. Keeping this idea in mind, we have designed and implemented a basic module with two ADCs and two DACs on board, with real-time and high-sensitivity characteristics, that could be easily integrated with the standard COTS. We included also a default connection link, keeping anyway the possibility of using any other connection link as a plug-in. The global architecture of this board started from the need of developing a modular card to be assembled in up to six copies on a single motherboard [2]. The motherboard hosts the default link, the main processor and a bus where the ADC/DAC modules can be connected. The ADC/DAC module has been designed, prototyped and tested on a NIOS development kit used as motherboard at the INFN in Napoli using Ethernet, RS232 and Enhanced Parallel Port (EPP - IEEE1284) to connect it to a PC. Then the communication logic has been embedded in the module's FPGA, and the module itself has been tested standalone in connection with a PC through a standard EPP. In this paper we discuss this

configuration and the performances of the system.

II. Preliminary studies

The idea of controlling a system by means of a hybrid system has been tested with a VME-UDP/IP based system as explained in [2]. If we define the Data Acquisition Time (ADC and DAC data conversion times), T_{DC}, the Data Transfer Time, T_{DT} and the Data Processing Time, T_{DP}, then the time necessary to generate the control signals from the acquired analog signals, T_{DM}, is:

$$T_{DM} = T_{DC} + 2 \cdot T_{DT} + T_{DP} < 1/f_c \qquad (1)$$

where f_c is the loop *control* frequency, which defines the maximum control band of the system. These parameters can be easily measured through simple application test: a known signal (e.g. a sine wave) with a fixed sampling frequency, f_s, is digitized by the ADC and sent through the link to the computing unit; the latter simply send it back to the DAC, that converts it again in an analogic signal. The input signal and the output signal are observed with an oscilloscope. It is easy to see in this test $T_{DP} = 0\,s$, so that the measured quantity is the Round Trip Time, $RTT = T_{DC} + 2 \cdot T_{DT}$, that is the time the whole system takes to convert, transfer through the chosen link technology and convert back the data. For what concerns T_{DP}, it is only possible to underline that it depends on the available computing power and on the complexity of the real-time computation. Nonetheless, taking into account the very high computing power of the state-of-the-art computing units, it can be considered negligigle with respect to T_{DC} and T_{DT} in most cases. The first tests performed with a VME-UDP/IP setup have shown that the control signal delay was approximately 2 samples at a maximum sampling frequency of $6.2\,kHz$ [2]. Since this result was quite far from our goals, we decided to test different protocols. We describe the architecture and the results in the following sections.

III. The integrated system

A. Concept and implementation

In order to make the hybrid acquisition and control more useful for on-field applications, we have developed a board that integrates all the functionalities of the control unit. This board (see Figure 1) is based on the Cyclone® (or Stratix®) family of Altera CPUs and the NIOS II® development kit. The main component of this board is a daughterboard containing two independent channels. The daughterboard has two $\pm 10\ V$ differential input and two differential $\pm 10\ V$ outputs on a load of $1\,k\Omega$. Each channel contains a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545) whose section A is used as Programmable Gain Amplifier (PGA) and section B to set the offset, a 20 bit DAC (Burr-Brown DAC1220) used for calibration and a 14 bit ADC to measure the internal temperature and allow an on-line correction. Each channel can be used either as a *fast* 16 bit DAC with a settling time of $0.5\,\mu s$ or as a 18 bit ADC with a maximum theoretical conversion rate of $2\,Msamples/s$ (for the first prototype a $800\,kHz$ ADC is used). Alternatively the channel can be used as a 18 bit

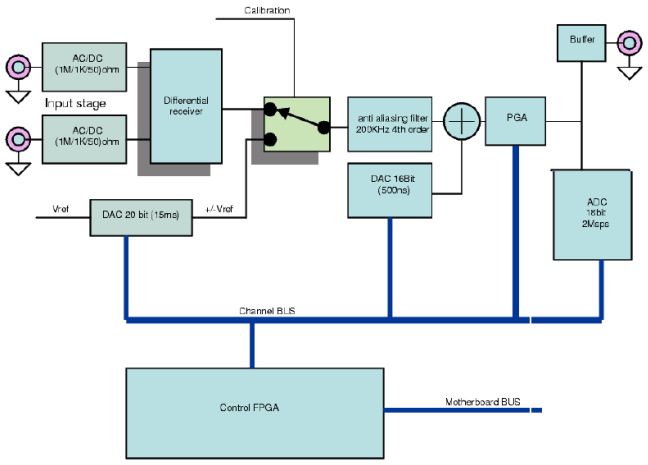


Fig. 1. Input channel schematics

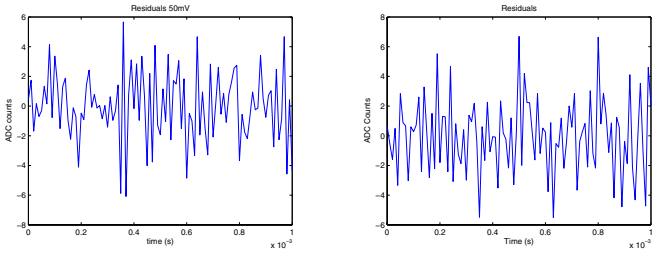
ADC and, at the same time, a 20 bit DAC with a settling time of $2\,ms$. The ADC trigger signal can be either internally generated on the daughterboard Programmable Logic Device (PLD) or taken from an external signal. An analogic 4^{th} order anti-aliasing filter is placed both on the input and the output path.

B. Performance tests

The first prototype, realized to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency. The NIOS kit was programmed in C language by means of the Altera© Quartus II® development software. The PLD on board the module was not used at all.

With this prototype, we performed tests on the ADC performance and on different communication links. To test the ADC, we simply acquired a sine wave with a $1\,kHz$ frequency and $50\,mV$ or $120\,mV$ peak to peak amplitude. A simple program on the NIOS, allowed the acquisition in memory of $1\,s$ of data and then transmit them to the PC through the RS232. We then evaluated the residuals of a fit with a sine function. The results are shown in figure 2. A value of ± 6 ADC counts, both at $50\,mV$ and $120\,mV$, results from the convolution of both the ADC and the generator precisions. Assuming 18 bits over a $\pm 10\,V$ scale, this means a precision of $12 \times 20\,V/2^{18} \sim 9.2 \times 10^{-4}\,V$, although it should be a function of the sampling frequency.

As far as the link tests are concerned, the fast Ethernet solution, as explained in [2], has produced very unsatisfactory results. We then tested the complete signal round-trip by using a Linux laptop connected with a RS232 port as computing unit, obtaining a maximum sampling frequency of $1.25\ kHz$ (see figure 3). We, then, decided to use the ADC-DAC module standalone, without the help of a motherboard, and to use a parallel port as communication link. The PLD on board the module has been programmed in VHDL in order to manage



(a) 50 mV (b) 120 mV

Fig. 2. Difference between the ADC read value and the input sine wave for $50\,mV$ and $120\,mV$ amplitude. The input sine wave estimation is the result of a fit.

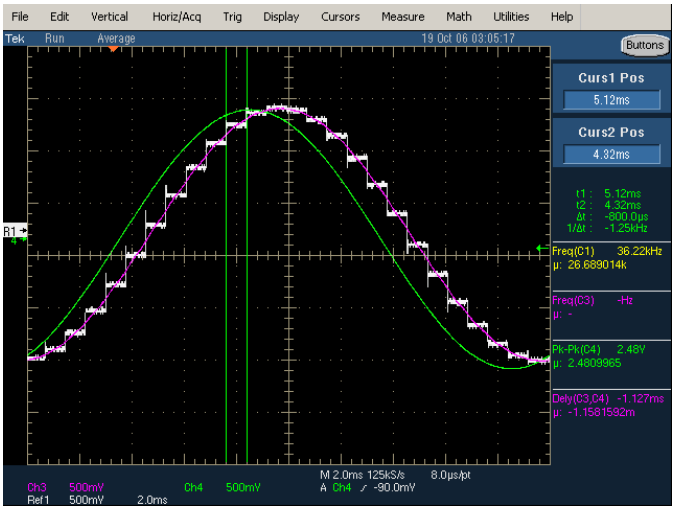


Fig. 3. Serial RS232 line test. The continuous line is the signal entering the ADC, the stepped the signal coming from the DAC. The continuous curve just below the DAC signal is an average over 1 second of the DAC signal. The sampling frequency is the step width and is determined by the link speed.

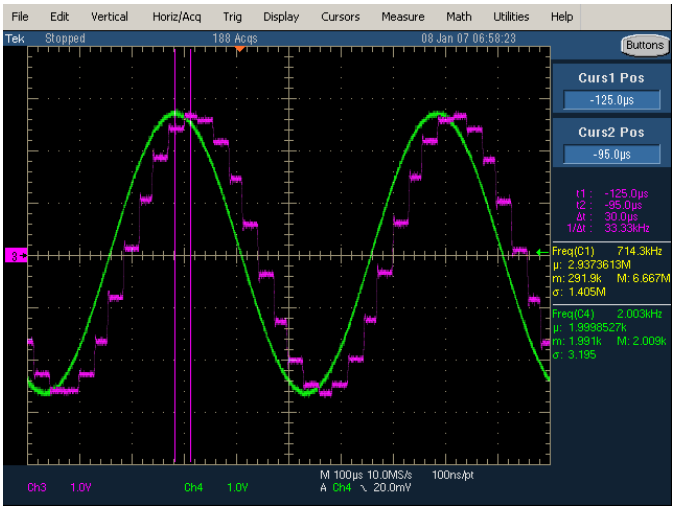


Fig. 4. Parallel EPP line test. The continuous line is the signal entering the ADC, the stepped one the signal coming from the DAC. The sampling frequency is the step width.

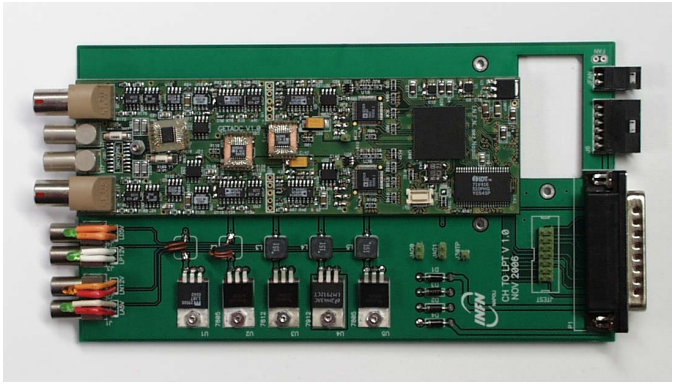


Fig. 5. The Prototype of the Module in standalone configuration. The hole in the power distribution base is to host the fan.

a protocol over an Enhanced Parallel Port (EPP), that allows programming and reading the internal module registers from the remote PC. The C language program used to program the NIOS development kit has been installed on the PC and adapted to use this protocol. This solution allows to driving only one module per parallel port. With this setup we again tested the complete signal round-trip, obtaining a maximum sustained sampling frequency of $\sim 40\,kHz$, although frequencies up to $80\,kHz$ could be reached if the time tag information is not enabled nor transmitted with data. In Figure 4 a test with a $33\,kHz$ frequency is shown.

This new *standalone* architecture gives also the possibility of acquiring samples at the maximum speed allowed by the ADC and of decimating the samples synchronously to an external trigger. To this purpose we developed on the board a digital moving average (MA) filter whose output is the average of the samples acquired between two trigger pulses, thus, for a trigger frequency of $10\,kHz$ and an ADC clock speed of $800\,kHz$, the acquired samples are the result of averaging $800/10 = 80$ ADC samples. In this way the same VHDL filter implementation can be used with any trigger frequency allowed by the communication link, while a more complicated filter would have required different numeric parameters for different frequencies.

To characterize the electronic and acquisition noises of the ADC, we acquired some seconds of data with the input closed on a $50\,\Omega$ termination, with and without the MA filter at different acquisition frequencies. Without the MA, we noticed a 10 LSB wide noise, while with the MA the *internal* noise is reduced to 2–3 LSB over the observed period at frequencies of 10 and $20\,kHz$, as can be seen in figure 6. In the same figure, it is possible to see a trend in the MA data, that can be interpreted as a temperature effect, as will be explained later in the paper.

A 14 bit ADC is also available to read an on board temperature sensor. The temperature information can be acquired by simply accessing a register to trigger it and two registers to read the ADC, without the need of a trigger pulse. In this way it is possible to correct the 18 bit ADC data with a dynamic calibration that takes into account the temperature drifts, by

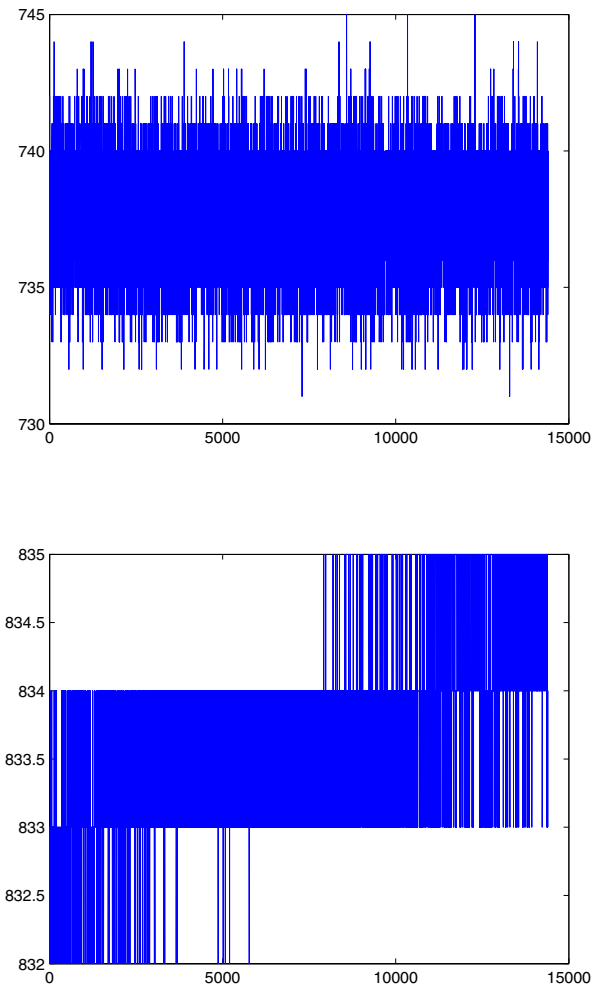


Fig. 6. Internal noise acquired at $20\,kHz$ raw and filtered with the Moving Average. The horizontal axis is the sample number, the vertical axis is ADC counts.

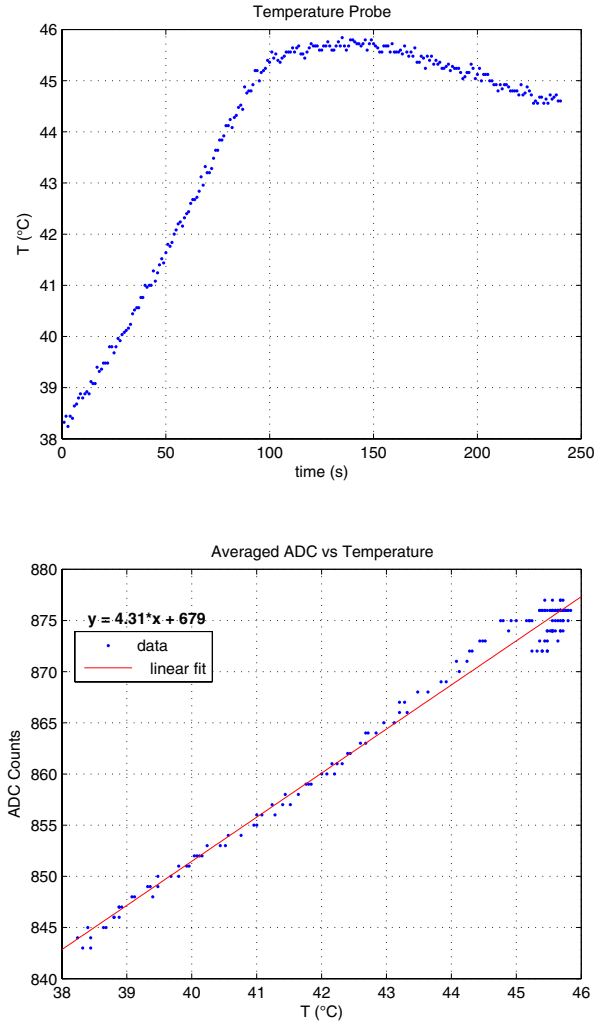


Fig. 7. Temperature vs time as measured by the on-board temperature probe and averaged ADC counts as a function of the temperature.

periodically acquiring the temperature information.

To test the effects of the temperature on the board, we placed it into an isolated heater and acquired the *terminated* input channel at different temperatures, using a moving average with a sampling frequency of $200\,Hz$. We noted that the ADC count is not linear with the temperature change, although it can be considered linear in intervals of about $5°C$. The fits show that the temperature coefficient assumes values in the interval from ~ 4.5 to ~ 6.5 $counts/°C$ in the range $40 - 55°C$. In figure 7, an example of the temperature measurements is shown.

Being these results very encouraging we are now designing and implementing a new prototype board with a $2\,MHz$ ADC with the same architecture described here.

IV. Applications

Although this device has been designed to be used in fast control systems such as laser interferometry controls, the co-existence in the same board of ADCs, DACs and external link makes this object very promising for many other applications. The system is now being extensively tested in two different R&D experiments, i.e. the read-out and control of a monolithic accelerometer with interferometric read-out in Salerno [3] and the control of the end mirrors of a suspended Michelson Interferometer through electrostatic actuators in Napoli. The latter is a prototype for mirror control for Interferometric Detectors of Gravitational Waves [4].

V. Conclusions

We have designed and prototyped a hybrid acquisition and control system with an on-board communication link. This solution allows the collection of data into a control station and the actuation/tuning on the basis of the collected data. The preliminary tests have shown that the developed system can sustain a sampling frequency of $f_c > 40\,kHz$ with a standard protocol over an Enhanced Parallel Port (EPP) and

can enhance its precision by using an oversampling/averaging filter. The system is now going to be extensively tested in two different experiments: i.e. read-out and control of monolithic accelerometer with interferometric read-out in Salerno and the control of the end mirrors a suspended Michelson Interferometer through electrostatic actuators in Napoli.

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