A Hybrid Modular Control and Acquisition System

Fabio Garufi, Fausto Acernese, Alfonso Boiano, Rosario De Rosa, Rocco Romano, and Fabrizio Barone

***Abstract*—In this paper we describe the architecture and the performances of a hybrid modular acquisition and control system prototype we developed in Napoli for distributed monitoring and control systems. The system, developed by our group within the framework of R&D for interferometric detectors of gravitational waves, is based on a dual-channel 18-bit low noise ADC and 16-bit DAC module at 800 kHz, managed by an Altera FPGA. The module is designed to be used standalone or mounted as mezzanine on a motherboard, in parallel with other modules. In particular, the modules can send/receive the configuration and the acquired/correction signal for control through a standard EPP parallel port to/from an external PC, where the real-time computation is performed. Experimental tests have demonstrated that this architecture allows the implementation of distributed control systems with a sustained sampling frequency up to $f_c \approx 80$ kHz, using a standard PC for the control signals computation. Each module is also equipped with a 20-bit slow ADC necessary for the acquisition of an external calibration signal. The system is now being extensively tested in on a prototype of suspended optical interferometer for gravitational wave detection we are developing at the INFN in Napoli, made of three superattenuators of the same class of the TAMA Interferometer.**

***Index Terms*—Data acquisition, real-time digital control.**

I. Introduction

THE design of digital control systems, both for industrial application and for R&D experiments, needs the definition of requirements on control band, sampling frequency, computing power, ADC and DAC characteristics. In many cases, the implementation of a control system becomes just a matter of choice of standards, technologies, control algorithms already described in literature or available on the market, often very reliable and effective. The design of non-standard control systems, like high performance control systems, adaptive control systems or distributed control systems is different. In this case the required large computing powers, distributed controlling actions, large control bands (of the order of kHz or larger) are not easily satisfied by commercial embedded or open systems, without using expensive and complex architectures (e.g., Digital Signal Processors (DSP) to be integrated in the acquisition and control system). The control system of the Interferometric Detector of Gravitational Waves Virgo [1], [2] is a typical example. In fact, this system is based on DSP VME boards designed and implemented to satisfy the specific requirements for computing power and data transfer of the Virgo detector control system. This solution, although very efficient, requires large investments, also in terms of manpower, for the design, implementation, test, maintenance and upgrade of the control system.

Therefore, a few years ago we decided to explore new possible directions of research in designing standard, low cost, high computing power and versatile digital control systems. The starting point of our approach is the requirement for a digital control system of a synchronous link among the different units (ADC, CPU and DAC). Actually, this requirement does not put any restriction on the protocol used for data transfer (synchronous or asynchronous) or on the operating system of the CPU, but states that all the operations of data transfer (ADC/CPU and CPU/DAC) and data processing must be always performed by the system in a time shorter than $t_c = 1/f_c$, where f_c is the digital control system sampling frequency. Therefore, it is, in principle, possible to link the acquisition/actuation units with the computing unit through standard commercial asynchronous protocols, although this solution seems to conflict with the *classical* requirement of a synchronous link among the units. But if the asynchronous data transfer is so fast that the sampling frequency is statistically guaranteed, then also an asynchronous link can be considered *synchronous* from the point of view of control theory. The advantage of this architecture is that the computing unit is completely independent from the acquisition/actuation unit, and, therefore, the computing unit can be chosen among a large variety of powerful and cheap standard technical solutions available on the market. In particular, the acquisition/actuation unit can be also a remote low-power system, equipped with a suitable link and a transmission protocol on board for connection with the computing unit. Finally, it is important to underline that this architecture still allows the use of the standard oversampling techniques for input digital noise reduction, since all the sampling operations are performed at the level of the acquisition/actuation unit. In the following we will refer to this class of control systems as *Hybrid Acquisition and Control Systems*. This technical solution, although in principle very simple and perfectly consistent with the basic theory of control systems, actually has never been implemented for control systems with control band larger than a few Hz.

In 2003 we began to study and test different technical configurations, aiming to demonstrate the feasibility of hybrid control

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F. Garufi and R. De Rosa are with the Istituto Nazionale di Fisica Nucleare, Sezione di Napoli, Complesso Universitario di Monte S. Angelo, I-80126 Napoli, Italy, and also with the Università degli Studi di Napoli Federico II, Dipartimento di Scienze Fisiche, Complesso Universitario di Monte S. Angelo, I-80126 Napoli, Italy (e-mail: fabio.garufi@na.infn.it; rosario.derosa@na.infn.it).

F. Acernese, R. Romano, and F. Barone are with the Istituto Nazionale di Fisica Nucleare, Sezione di Napoli, Complesso Universitario di Monte S. Angelo, I-80126 Napoli, Italy, and also with the Università degli Studi di Salerno, Dipartimento di Scienze Farmaceutiche, I-84084 Fisciano (Salerno), Italy (e-mail: fausto.acernese@na.infn.it; rocco.romano@na.infn.it; fabrizio.barone@na.infn.it).

A. Boiano is with the Istituto Nazionale di Fisica Nucleare, Sezione di Napoli, Complesso Universitario di Monte S. Angelo, I-80126 Napoli, Italy (e-mail: alfonso.boiano@na.infn.it).

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systems with sustained sampling frequencies, f_c, of the order of 100 kHz [3]. This is the requirement on the digital control sampling frequency of a prototype of suspended optical interferometer we are developing at the INFN–Napoli for R&D on the second generation of interferometric detectors for gravitational waves, that is $f_c = 10$ kHz (the same frequency of the Virgo control system). The complexity of the digital control system is due to the fact that the optical interferometer prototype consists of three superattenuators of a new generation, similar to the ones installed in the TAMA Interferometer [4], [5], and requires a distributed control characterized by many inputs and outputs, a large computing power and the typical ADC/DAC resolution of the interferometers for gravitational wave detection. The requirement of a sustained sampling frequency of one order of magnitude larger than the effective requirement of $f_c = 10$ kHz is a further guarantee that the hybrid control system will be also statistically robust.

The implementation of a hybrid control system requires the choice of acquisition/actuation units with suitable communication channels. Many ADC/DAC boards are available on the market for the vibration monitoring and suppression (see e.g., [6], [7]), but not suitable for our purposes because of the ADC and DAC limited resolution and the lack of a standard communication link, being conceived to work together with DSP boards or inside a PC. Other solutions with higher resolution (e.g., [8]), typically used in audio systems, make use of $\Sigma - \Delta$ ADCs that are not suitable to follow slowly variable signals, as those that we must monitor to control the interferometer suspensions. For this reason we developed a modular board with a 18 bit Successive Approximation (SAR) ADC, a 16 bit DAC and a communication channel that permits to connect the board to the standard I/O ports available on present day PCs without the need of using a specifically designed solution and capable to achieve a control frequency band up to tens of kHz. The complete project foresees the implementation of a modular ADC/DAC card to be assembled in up to six copies on a single motherboard [9], that should host the default link, the main processor and a bus where the ADC/DAC modules can be connected. Since in this architecture there is only one communication link for all the channels, a channel identifier is scheduled to be coded into the transmitted data. The different modules will be read at different times, so that it would be possible to transmit a time tag together with each ADC data. The implementation of the motherboard has not yet started and has be postponed to the completion of the final tests we are performing on the suspension control of the optical interferometer prototype in Napoli.

The first prototype of the ADC/DAC module has been designed, prototyped and tested, connected with a specifically designed interface to a NIOS development kit [10] used as a simulation of the motherboard. With this set-up we tested the behaviour of the hybrid acquisition and control system with Ethernet, RS232 and Enhanced Parallel Port (EPP – IEEE1284) connected to a PC [11]. The best results were obtained using a standard EPP, that allows to sustaining a control frequency of ($f_c \approx 80$ kHz), that is very close to our final goal.

We also considered the possibility of using the ADC/DAC module without an intelligent motherboard. For this purpose, the communication logic has been embedded in the module's FPGA, and the module itself has been tested standalone in connection with a PC through a standard EPP.

In this paper we discuss the architecture, the configuration, the performances and the applications of this hybrid digital control system.

II. Preliminary Studies

A. The Model

In the following we will describe the model we used to demonstrate the theoretical feasibility of a hybrid digital control system. If we define the Data Acquisition Time (ADC and DAC data conversion times), T_{DC}, the Data Transfer Time, T_{DT} and the Data Processing Time, T_{DP}, then the time T_{DM} necessary to generate the control signals from the input analog signals, is

$$T_{DM} = T_{DC} + 2 \cdot T_{DT} + T_{DP} < \frac{1}{f_c} \tag{1}$$

where f_c is the sampling frequency (i.e., the loop *control* frequency), which defines the maximum control band, B, of the system (typically $B < f_c/10$), assuming a symmetrical communication link and the same amount of data in both directions. The T_{DM} parameter can be easily measured through a simple application test: a known signal (e.g., a sine wave) with a fixed sampling frequency, f_c, is digitized by the ADC and sent through the link to the computing unit; the latter simply sends it back to the DAC, that converts it again to an analogic signal. The input signal and the output signal are observed with an oscilloscope. It is easy to see that in this test $T_{DP} = 0$ s, so that the measured quantity is the Round Trip Time, $RTT = T_{DC} + 2 \cdot T_{DT}$, that is the time the whole system takes to convert, transfer through the chosen link technology and convert back the data. For what concerns T_{DP}, it is only possible to underline that it depends on the available computing power and on the complexity of the real-time computation. Nonetheless, taking into account the very high computing power of the state-of-the-art computing units, it can be considered negligible with respect to T_{DC} and T_{DT} in most cases. On the other end, the quantity $2 \cdot T_{DT}$, can be evaluated independently with a network-only test where a packet is generated in the acquisition unit, sent to the computing unit and sent back to the acquisition unit.

B. Preliminary Tests

The first general tests on the hybrid architecture were performed with an VME-UDP/IP based system, derived from an already existing system originally used for developing software for tests on digital control systems for a VIRGO R&D program [3], [9]. The goal was to replicate the performance of the existing system with the new architecture. In this first set-up the acquisition and control unit was composed of a VME Single Board Computer (SBC) with a hard real-time operating system (LynxOS 4.0),[1] a 32 channel VME ADC and a 16 channel VME DAC. The SBC used the on-board fast Ethernet link as the communication link with a 2 GHz Intel Linux PC used as computing unit.

[1]LynxOS is a registerd mark of LynuxWorks: 855 Embedded Way, San Jose CA 95138-1018.

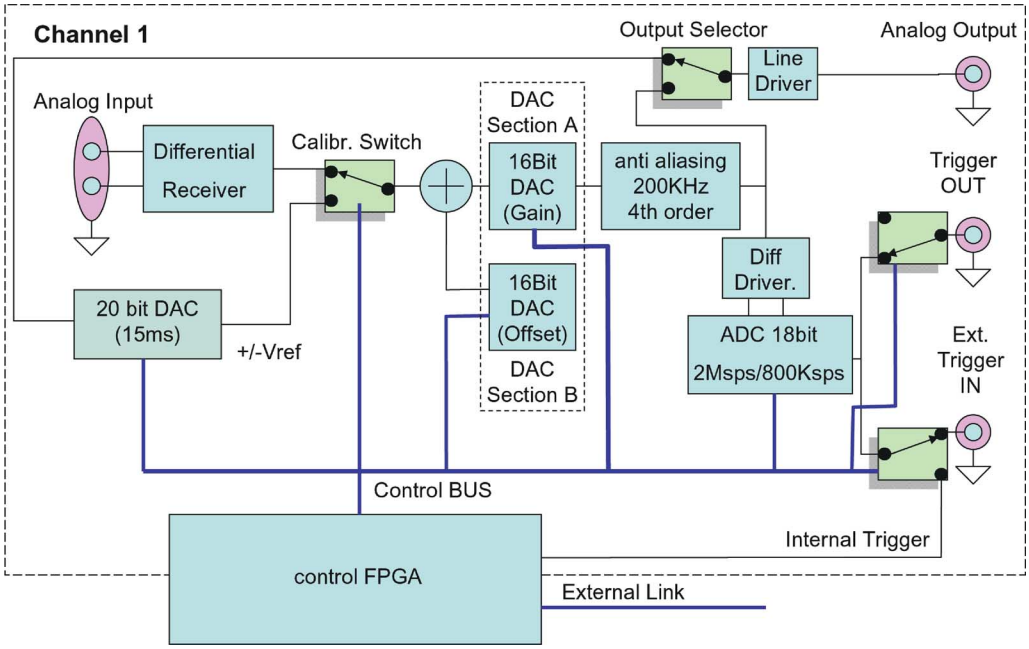

Fig. 1. Block scheme of the acquisition and control daughterboard. In the picture only one channel is shown, being everything but the FPGA duplicated for the other channel. The switches connected to the control bus are managed by FPGA registers, the output selector is set via a jumper. The ADC trigger can be either internally or external generated and, in both cases, can be routed to an output connector.

The first tests performed with this VME-UDP/IP setup have been just the simple acquisition-actuation round-trip described in the previous subsection and presented a control signal delay of ≈ 2 samples at a maximum sampling frequency of 6.2 kHz [3], [9] although the simple UDP packet round-trip test gave times in the 240 μs range. Since the result on the acquisition-actuation test was quite far from our goal of $f_c = 100$ kHz, we decided to replicate the network based tests on the module prototype and to test different protocols.

We will describe the architecture and the results in the following sections.

III. Module Prototype

A. Concept and Implementation

In order to make the hybrid acquisition and control useful for field applications, we have designed a daughterboard prototype, integrating all the functionalities of an acquisition and control unit. The board, based on the Cyclone family of Altera Programmable Logic Devices (PLD), has been developed with the help of the NIOS II development kit [10], an integrated board providing a hardware platform for developing embedded systems based on Altera Cyclone II devices. It also provides an on-board Ethernet MAC/PHY device and RJ45 connector, RS-232 DB9 serial port, JTAG connectors to Altera devices via Altera downloads cables.

While the full project would consist of a motherboard hosting multiple copies of the acquisition and control daughterboard, we are currently working only on the prototype of daughterboard. The daughterboard prototype (see Fig. 1) hosts a Cyclone EP1C6F256C6 FPGA and two independent channels (± 10 V differential input–differential ± 10 V outputs on a load of $1\text{k}\Omega$). Each channel consists of a 18 bit ADC (AD7641), a dual 16 bit DAC (AD5545), a 20 bit DAC (Burr-Brown DAC1220). The two 16 bit DACs (called Section A and Section B) have different purposes in the input and output paths. In the input path, Section A is used as Programmable Gain Amplifier (PGA) and Section B is used to set the offset of the 18 bit ADC, while in the output path Section A is used to set the output channel gain, while Section B is used to set the output. This implies that a channel can be used as either an input channel or as an output one. Each channel can be used instead either as a *fast* 16 bit DAC with a settling time of 0.5 μs or as a 18 bit ADC with a maximum theoretical conversion rate of 2 Msamples/s (for the first prototype a 800 kHz ADC is used). Alternatively each channel can be used as a 18 bit ADC and, at the same time, a (slow) 20 bit DAC with a settling time of 2 ms. The ADC trigger signal can be either internally generated on the motherboard or daughterboard PLD or taken from an external signal: both the internally generated and the external trigger pulses can be routed to an output connector. An analogic 4th order anti-aliasing filter is placed both in the input and the output path. A 14 bit ADC (internal to AD7641) is used to read the board temperature for on-line correction.

The advantage of this board compared to other similar systems available on the market, is the possibility of having a control band that can span continuously from mHz to tens of kHz, without the need of large oversampling. Other systems, based on $\Sigma - \Delta$ ADCs, are faster and more efficient on the high frequency range, but fail with slowly varying (< 100 Hz) signals.

Mechanically, the module is conformant to a 2U Eurocard with a 60 pin 0.5 mm pitch bus connector on the face opposite to the component side, providing the interface with the motherboard and/or a power supply and external link board. The motherboard, still in a preliminary design study phase, should be a 6U Eurocard with the possibility to mount VME connectors to obtain the power supply from the VME power lines.

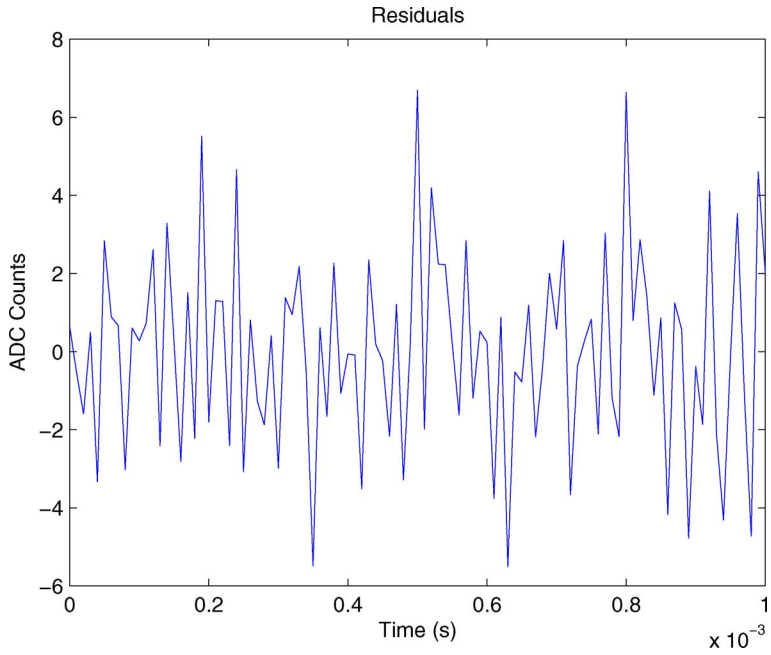

Fig. 2. Difference between the ADC read value and the input sine wave for 120 mV amplitude. The input sine wave estimation is the result of a fit. The maximum value of the residual is a result of the sampling step and the input signal slope.

B. Performance Tests

The first prototype, built to test the idea of the multiple boards on a motherboard, used the NIOS Cyclone development kit to emulate the motherboard, to manage the external link communication and to generate a programmable clock frequency.

The NIOS kit was programmed in C language by means of the Altera Quartus II development software. The PLD on board the module was not used at all.

The data stream to the PC is composed of a sequence of 3 words of 32 bit per ADC sample: the first 2 words represent an internally generated time tag and the third the ADC data. For both ADC and time tag words, of the 32 bits, the most significant, if set, indicates that the data FIFO is empty, the 18 least significant the data value, the remaining are used to identify the module in case more than one is present on the motherboard, and if the data are ADC or time tag. By reading the data FIFO register at the maximum speed allowed by the communication link and looking at the most significant bit the last converted data is read at the maximum speed.

With this prototype, we performed tests on the ADC performance and on different communication links. At this level of development the most important goal was the demonstration of the feasibility of the whole architecture.

1) ADC Performances: The purpose of the tests on ADC we performed is only to verify at this state the correct functioning of the board and to have a rough idea of the ADC resolution.

To test the ADC, we simply acquired a sine wave with a 1 kHz frequency and 50 mV or 120 mV peak to peak amplitude. A simple program on the NIOS, allowed the acquisition in memory of 1 s of data and then transmit them to the PC through the RS232. We then evaluated the residuals of a fit with a sine function. The results at 120 mV are shown in Fig. 2. A value of ± 6 ADC counts, both at 50 mV and 120 mV, results from the convolution of both the ADC and the generator precisions.

Fig. 3. Prototype of the module with the power distribution board. The hole in the power distribution base is to host the fan.

Assuming 18 bits over a ± 10 V scale, this means a precision of $12 \times 20\ \mathrm{V}/2^{18} \sim 9.2 \times 10^{-4}$ V, although it should be a function of the sampling frequency and of the input signal slope.

2) Integrated Tests: The complete signal round-trip test with a Linux laptop with a Intel Centrino 1.8 GHz CPU as computing unit, connected with a RS232 port, has given a maximum sampling frequency of 1.25 kHz. The ADC sampling clock pulse used in this test has been both internally and externally generated, with no substantial difference.

Then the NIOS kit FPGA has been programmed in VHDL to use some output pins to manage a protocol compatible with an Enhanced Parallel Port (EPP) on a personal computer. The ADC-DAC module has been finally tested standalone, without the help of the NIOS kit, and using a parallel port as communication link. The PLD on-board the module has been programmed in VHDL in order to manage a protocol over an Enhanced Parallel Port EPP, that allows programming and reading the internal module registers from the remote PC. For these tests, a power distribution board hosting the parallel port D25 connector, low

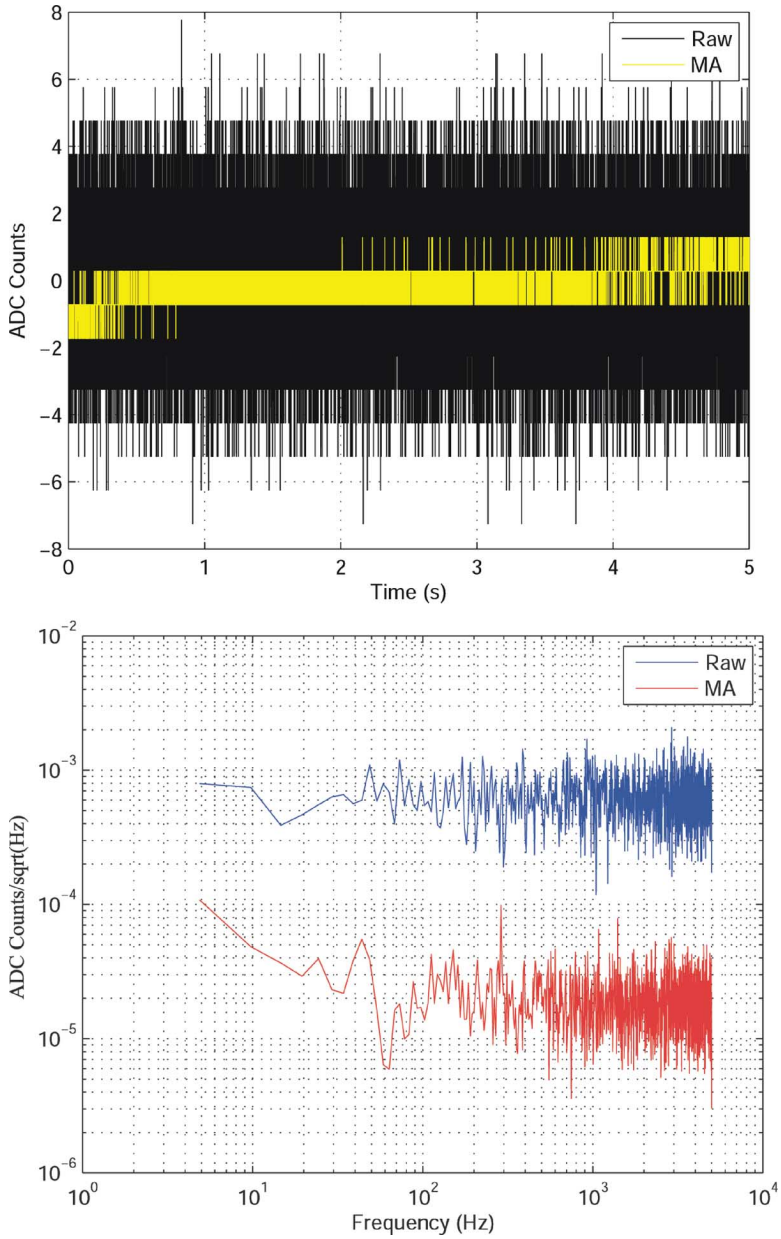

Fig. 4. Internal noise acquired at 10 kHz raw and filtered with the moving average and power spectral density of the two data series. The moving average operation lowers the noise level of a factor $\sim 10^2$ at this frequency ($1 \text{ count} = 20 \text{ V}/2^{18}$).

noise voltage regulators and the data and power lines has been designed. The C language program used to program the NIOS development kit has been installed on the PC and adapted to use the EPP protocol. This solution allows to drive only one module per parallel port. A picture of the module is shown in Fig. 3. With this setup we again tested the complete signal round-trip, obtaining a maximum sustained sampling frequency of ~ 40 kHz, although frequencies up to ~ 80 kHz were reached when the time tag information was not enabled nor transmitted with data.

3) Noise and on Board Filter Tests: The VHDL program used in this new *standalone* architecture gives also the possibility of acquiring samples at the maximum ADC speed and filling the data FIFO with the last acquired sample synchronously to an external trigger. To this purpose we developed on the board a digital moving average (MA) filter whose output is the average of the samples acquired between two trigger pulses, thus, for a trigger frequency of 10 kHz and an ADC clock speed of 800 kHz, the acquired samples are the result of averaging $800/10 = 80$ ADC samples. In this way the same VHDL filter implementation can be used with any trigger frequency allowed by the communication link, while a more complicated filter would have required different numeric parameters for different frequencies.

To characterize the electronic and acquisition noises of the ADC, we acquired some seconds of data with the input closed on a 50 Ω termination, with and without the MA filter at different acquisition frequencies. Without the MA, we noticed a ~ 10 LSB wide noise, while with the MA the *internal* noise is reduced to 2–3 LSB over the observed period at frequencies of 10 and 20 kHz, as can be seen in Fig. 4. In the same figure, it is possible to see a trend in the MA data, that can be interpreted as a temperature effect, as will be explained later in the paper.

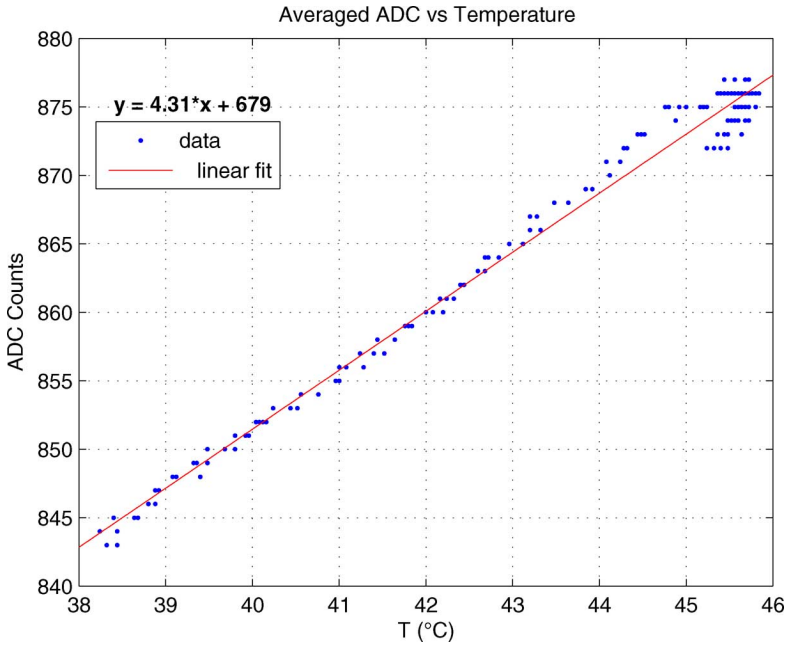

Fig. 5. Value read by 18 bit ADC on a 50 Ω load versus the temperature read by 14 bit ADC reading the on-board temperature probe. The board has been placed into an electric oven and the measurements have been taken every second while the oven temperature was rising.

A 14 bit ADC is also available to read an on board temperature sensor. The temperature information can be acquired by simply accessing a register to trigger it and two registers to read the ADC, without the need of a trigger pulse. In this way it is possible to correct the 18 bit ADC data with a dynamic calibration that takes into account the temperature drifts, by periodically acquiring the temperature information.

To test the effects of the temperature on the board, we placed it into an isolated heater and acquired the *terminated* input channel at different temperatures, using the moving average filter with a sampling frequency of 200 Hz. We noted that the ADC count is not linear with the temperature change, although it can be considered linear in intervals of about 5°C. The fits show that the temperature coefficient assumes values in the interval from ~ 4.5 to ~ 6.5 counts/°C in the range 40 °– 55 °C. In Fig. 5, an example of the temperature measurements is shown.

IV. Applications

The system was extensively tested in the longitudinal control from the reference mass of the end mirror of the lower stage of a suspended Michelson interferometer through electrostatic actuators, as part of the digital control system of the prototype of the suspended optical interferometer, consisting of three superattenuators of the same class of the TAMA Interferometer [4], [5], we are developing at the INFN–Napoli for R&D on interferometric detector of gravitational waves of second generation. The optical set up is shown in Fig. 6. The sampling frequency is $f_c = 10$ kHz [11], [12].

The first arm optics is mounted on the lower stage of a double pendulum suspension. The position of its upper stage is controlled in both rotational and longitudinal degrees of freedom using coil-magnet actuators. The second arm end with a mirror suspended to a similar double pendular suspension. The upper stage is controlled in all degrees of freedom by means of coil-magnet actuator. For both upper stages the digital control is achieved by using a standard VME ADC-CPU-DAC architecture.

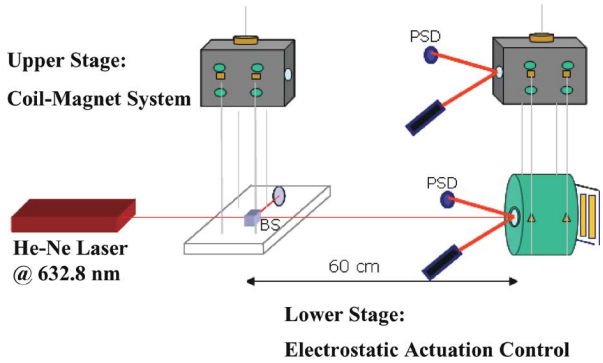

Fig. 6. Suspended Michelson interferometer.

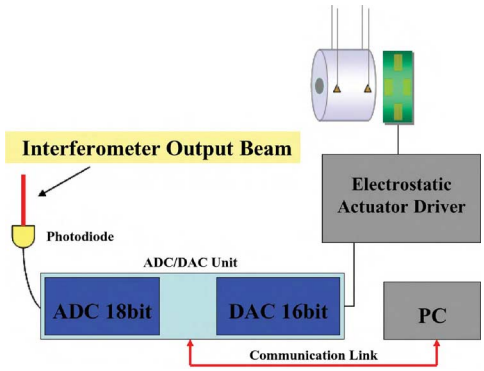

Fig. 7. Lower stage control system architecture.

In the lower stage (Fig. 7) the mirror tilts are controlled with classical optical levers, consisting of laser and position sensing diodes (PSD), while the mirror longitudinal motion is instead

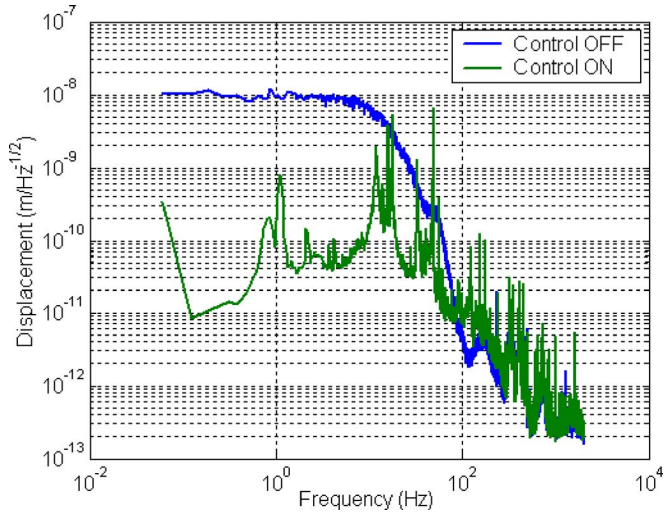

Fig. 8. Preliminary results of the suspension lower stage control with electrostatic actuators. The power spectral density of mirrors' relative displacement are shown both with and without the lower stage control. The peaks in the controlled power spectrum are due to residual mechanical rotational-translational modes coupling and violin modes.

controlled, through electrostatic actuators, with the 18 bit hybrid digital control system, that replaces the Virgo like VME based digital control originally used in the prototype of the suspended interferometer in Napoli. The lock of the interferometric system is easily achieved. Preliminary results displayed in Fig. 8 show that the control is capable of a reduction of two orders of magnitude in the mirror displacement noise in the mHz–10 Hz frequency band, that is what we expected from the theoretical simulation of the control system. The presence of peaks in the controlled power spectrum is due to the coupling of the residual mechanical rotational-translational modes of the suspensions and to the violin modes of the suspension wires. Although these results can be, of course, improved, partly with a more refined design of the control strategy, they show no limitation due to the hardware used for the longitudinal control, demonstrating that a classical Virgo like VME based digital control can be replaced by a hybrid digital control system on a mechanical suspension developed for interferometric detectors for gravitational waves, keeping the same sampling frequency of 10 kHz.

V. Conclusion

We have designed and prototyped a hybrid acquisition and control system with an on-board communication link. The preliminary tests have shown that the prototype module coupled with a PC unit can sustain a sampling frequency ranging from the continuous region up to $\approx f_c = 80$ kHz with a standard protocol over an Enhanced Parallel Port (EPP), with an enhanced precision by using an oversampling/averaging filter. The system is being now extensively tested in the longitudinal control from the reference mass of the end mirror of the lower stage of a suspended Michelson interferometer through electrostatic actuators, as part of the digital control system of the prototype of the suspended optical interferometer we are developing at the INFN–Napoli for R&D on interferometric detector of gravitational waves of second generation, with a sampling frequency of $f_c = 10$ kHz, with satisfying results. As these results are very encouraging we are now designing and implementing a new daughterboard prototype board with a 2 MHz ADC with the same architecture described here, aimed to test also other possible communication protocols.

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