

# The Data Acquisition and Transport Design for NEMO Phase 1

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**Abstract**—The NEMO collaboration proposes to build an underwater neutrino telescope located South-East off the Sicily coast. This paper describes the concepts underlying the communication link design going over the whole data acquisition and transport from the front-end electronics to the module sending data on-shore through a fiber optic link which relies on Dense Wavelength Division Multiplexing. An on-shore board, plugged into a PC, extracts and distributes data both to first-level trigger and control systems. Underwater apparatus monitoring

and controls are guaranteed by oceanographic instruments and dedicated sensors, whose data are packed and sent back to shore using the same optical link. The communication is fully bidirectional, allowing transmission of timing and control commands. The architecture described here provides a complete real-time data transport layer between the onshore laboratory and the underwater detector. During winter 2006 a first prototype of the apparatus has been deployed: calibration results from the currently working system are here reported.

## I. INTRODUCTION

**T**HE NEMO collaboration [1] aims at the construction of an underwater neutrino telescope which could be located about 80 km SE off the Sicily coast at about 3500 m depth [2]. Neutrino telescopes (see references to similar projects [3], [4], [5], [6], [7], [8] and [9]) point at the reconstruction of physical events generated by high-energy astrophysical neutrinos interacting with matter. The underwater apparatus relies on the detection, by means of photomultipliers (PMT), of Čerenkov light due to the propagation, in water, of relativistic charged particles originated by the neutrino interaction. Photons hitting the PMT generate electrical signal pulses, called “hits”: the readout goal consists of measuring the time at which the hits originated and some information related to the charge and to the pulse shape.

Two main considerations have a deep impact on data transmission architecture: the presence of an average hit rate and the necessity of distributing a common timing. The first one is mainly due both to PMT dark current and, for an apparatus deployed in the sea, to natural background comprising  $^{40}\text{K}$  decays and, depending on the specific site properties, some level of bioluminescence. As shown by previous measurement campaigns [10], [11], [12] and theoretical calculations [13], a 10” PMT, with a dark current of few kHz, is expected to show a background rate of about 50 kHz with a threshold set to half of a single photo electron (*spe*) pulse height in the site proposed for the km3 apparatus. In addition, the average hit rate in the NEMO test-site is increased by bio-luminescence up to  $\sim 80$  kHz. Most of the hits can be thought of as produced by *spe* signals, which are characterized by an amplitude of about 120 mV and a duration of 8 ns for the chosen PMT.

Regarding the timing issue, each signal must be labeled by a “time stamp”, i.e. the hit arrival time, in order to reconstruct tracks. This statement implies that each readout electronics, whatever its design, needs common timing and known delay with respect to a fixed reference. Thus, either an absolute time or, at least, the phase offset between time stamps produced by different readouts must be measured. This time alignment is the task of the *timing calibration* procedure, which can be effectively eased endowing the whole electronics system of specific features like deterministic latency. The required time resolution of the readout system must be less than 1 ns to allow track reconstruction with optimal angular resolution.

The proposed mechanical layout of the experiment consists of 81 towers equispaced on a 150-200 m lattice grid; each tower is 700 m high and hosts up to 18 *floors* whose arms are about 12 m long. At each arm end a pair of glass spheres are placed, containing the so-called Optical Module (OM), consisting of a PMT with its power module and a readout electronic board. Thus, the minimal self-consistent structure in the whole apparatus design is the tower.

During winter 2006 a *mini-tower*, equipped with 4 floors and schematically shown in Fig. 1, was deployed for the pilot experiment called *NEMO Phase I* in the NEMO test-site, about 25 km off the Catania port at a depth of 2000 m. Floor power and fibers are extracted from the electro-optical backbone by proper devices placed inside the *breakout* vessel (br). The floor

electronics is powered by the Floor Power Module (FPM). All floor devices communicate with the on-shore laboratory through the Floor Control Module board (FCM): the main components are the Optical Modules (OM), the oceanographic instruments used to measure water current (ADCP), water transparency ( $C^*$ ), sea water properties (CTD); acoustic positioning is implemented using a pair of hydrophones (H) placed at each arm end. The tower electro-optical cable can be connected to the main cable, which arrives from on-shore, by a submarine operable connector (HC).

Even though the number of floors is reduced, the functionalities of the full tower are preserved, as far as possible, to have the deepest insight into the final system. In fact, the design of the mini-tower permitted us to test scalability issues in order to allow a progressive enlargement of the experiment just adding more and more towers. Fig. 2 shows the basic scheme of the floor data acquisition and communication system. Each floor is independent of the others and is connected by an optical bidirectional point-to-point link (indicated as (2)) to shore<sup>1</sup>. The PMT measurements and the monitoring data, produced by front-end boards, are collected by the FCM, packed together and transmitted through the optical link; control data are received from on-shore following the opposite direction. The on-shore host machine, called Floor Control Module Interface (FCMI), can be accessed through a Gigabit Ethernet (GbE) connection.

Other considerations, related to the hostile experimental

<sup>1</sup>Actually the link is put into effect by means of *add & drop* passive devices which mux/demux more optical channels at different wavelengths into/from the same fiber. For the sake of brevity the reader is addressed to reference [14].

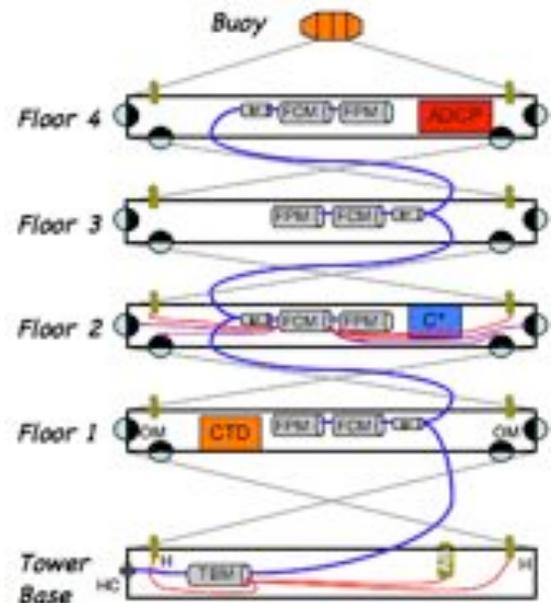


Fig. 1. Fully equipped NEMO Mini-Tower pictorial view; the Floor Control Module (FCM), roughly placed at the floor center, is powered by the Floor Power Module (FPM) and connected to the on-shore lab through a fiber optic backbone. All floor devices are connected to the FCM: Optical Modules (OM), Oceanographic Instrumentation to measure water current (ADCP), water transparency ( $C^*$ ), sea water properties (CTD), and a pair of hydrophones (H) for acoustic positioning.

environment, affect project choices: submarine technology at the targeted depth is very challenging and the use of cables, connectors, and penetrators to transport data, controls, and power is a difficult and expensive task. Electronics design is, then, required to minimize connections, limit power consumption to a couple of watts per channel, and reduce physical dimensions in order to simplify the mechanical layout of the apparatus and diminish the volume of the vessels which support very high pressure.

In section II the communication protocol and its impact on the whole project will be discussed. The Front End Module (FEM) board designed for underwater PMT signal acquisition will be shown in section III; then the FCM board will be dealt with in section IV. The same FCM board is used on-shore to establish a connection with off-shore electronics and distribute data to the next DAQ levels. Some insight into timing calibration issues will be given in section V. Finally, preliminary results coming from the currently running apparatus will be presented in section VI.

## II. SYNCHRONOUS PROTOCOL FOR DATA TRANSPORT

The common timing needed over the whole apparatus scale and the average hit rate advised us to choose a synchronous protocol, which embeds the clock signal in the transmitted bit stream, to exchange information between on- and off-shore. The receivers on both ends can recover clock and data and can provide a timing reference synchronous by design with the transmission clock. This choice reduces the number of physical links needed to transfer data: since a reasonable number of fibers per cable is limited to some tens, fewer connections mean higher reliability, easier scalability, lower costs, and a simpler deployment.

Beyond the choice of a synchronous link, a constant and fixed latency is also needed to guarantee that receivers are able to output the same serial input at the same time. This property is not cared for by usual telecommunication systems,

because unknown and random latencies on the order of few nanoseconds can be neglected, but in real time experiments, where “time stamping” is one of the main tasks, this feature assumes a vital role. Both the synchronous and fixed latency properties must be assured by the protocol implementation with sub-nanosecond precision, which is the target value set to obtain the desired angular resolution for event reconstruction. These items will be dealt in more detail in section V.

To implement the protocol, we chose a commercial chip set consisting of a transmitter and a receiver pair of distinct ICs, the HDMP-1032 and HDMP-1034 formerly developed by Hewlett Packard and now produced by PMC-Sierra [15]. They can be used together to realize a high-speed point-to-point serial link. As claimed by the producer, the chip set can be seen as a “virtual ribbon cable”, in the sense that parallel words on the transmitter side are sent and reproduced at the receiver side without any user intervention regarding physical layer complexity. For an exhaustive description of the chip set details, the reader is addressed to [16].

A unique timing station, synchronized with a GPS receiver, provides the clock to the on-shore electronics which transmits data to off-shore, as explained later in section V. The clock recovered underwater at the floor level is distributed to all the devices needing a timing signal so as to make each single part of the system synchronous.

With a maximum parallel clock frequency of 70 MHz and a 20 bit transmitted word (with only 16 bits available to the user), the chip set allows a data rate of up to 1.4 Gbps, with a maximum user payload of 1.12 Gbps. For this project we chose a system clock of 40 MHz yielding a payload of 640 Mbps. This bandwidth is abundantly higher than required by data produced at floor level which is limited to 100 Mbps. Even considering some room to integrate other control devices such as environmental sensors, control for the calibration board, data from hydrophones (which could be even as demanding as the Optical Modules readout electronics), the available payload is still large enough to accommodate the expected data.

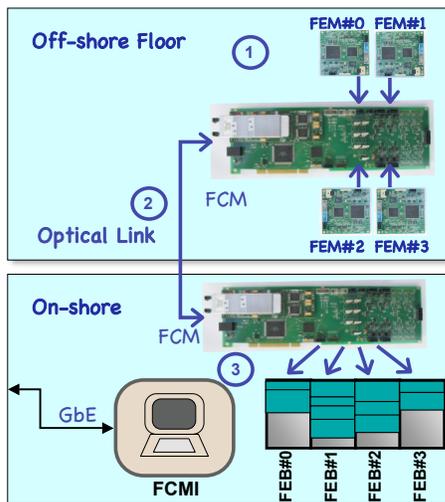


Fig. 2. Scheme of on-shore/off-shore point-to-point link: PMT data digitized by front-end boards (FEM) are collected by the FCM, transmitted to on-shore, written to PC memory areas called Front-End Buffers (FEB), and distributed through GbE interface.

## III. THE FRONT END MODULE

The Front End Module board is placed close to the PMT inside the glass sphere that contains the whole Optical Module. The FEM digitizes the analog signals produced by the PMT, encoding and transmitting these data in a suitable way to the FCM.

The starting design choice for data acquisition was to digitize and transmit the hit waveform. In Fig. 3 the FEM picture is shown: the PMT signal is carried over a coaxial cable and conditioned by the *Analog Front End*; then the signal is sampled, digitally converted and eventually stored by an FPGA. Board control is accomplished by the Digital Signal Processor (DSP). Another block is dedicated to communication with the FCM.

We considered a resolution of 8 bits and a sampling frequency of 200 MHz capable to retain all interesting information still allowing a good compromise between performance and power consumption. To push even further the power saving strategy, the signal is sampled using two 8-bit Fast Analog

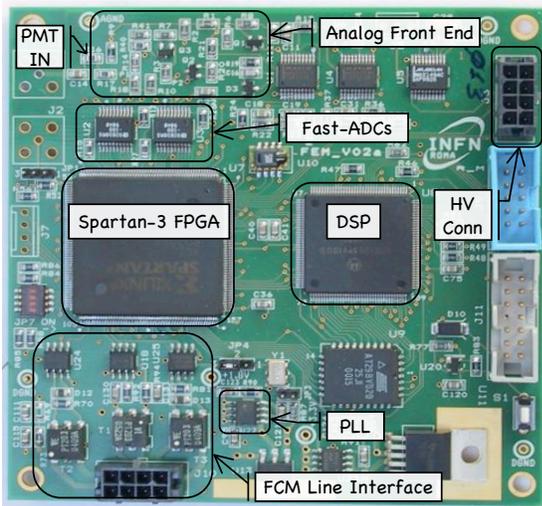


Fig. 3. FEM board picture: PMT signal is conditioned, digitized by ADCs, and transmitted to FCM.

to Digital Converters (Fast-ADCs) running at 100 MHz but staggered by 5 ns: this technique gives the desired sampling rate yet allowing a lower power dissipation than a single 200 MHz ADC<sup>2</sup>.

To comply to Nyquist theorem, the PMT signal is band-limited by an anti-aliasing filter which stretches the spe pulse to 50 ns. To match the  $[0 \div -5 \text{ V}]$  input dynamic range to the 1.024 V input voltage range of the ADCs, the signal level is shifted and compressed by a non-linear circuit, which applies a quasi-logarithmic law. The equivalent resolution obtained amounts to about 13 bits with a constant relative error. In order to find out the compression characteristic curve a self-calibration circuit is used: analog levels are generated by an on-board 12-bit digital to analog converter, fed to the compressor circuit and then sampled by the Fast-ADCs. After data analysis and previous linear components measurement, a lookup table, representing the whole amplitude response from input signal to ADCs, can be determined. To exploit the small ADCs dynamic range, the offsets must be appropriately set by a 12-bit digital to analog converter, so that the minimum input voltage (0 V) corresponds to a low ADC value, in order to avoid ADC channels wasting.

The electric signal is continuously sampled by the two ADCs and the two bytes (referred to as a word) are fetched at a frequency of 100 MHz by the FPGA. Two digital comparators continually check the input word: if one of the two bytes exceeds a programmable threshold, dynamically set by the user, the hit is stored in a FIFO inside the FPGA. If neither of the two bytes is over threshold the word is discarded. When an over-threshold word is found, indicating the hit start, the following pieces of information are stored: the threshold time (which is the sampling time, counted by a 16-bit 100 MHz counter, of the word passing the threshold), 2 or 3 *pre-trigger* samples (amplitude values before the threshold

time), and the hit samples. Data are continuously stored until a programmable number of words is under threshold. This feature makes possible studying the signal pedestal, merging *after-pulse hits* into a single hit<sup>3</sup> or optimizing the hit size with respect to fixed length samplers. This procedure, which discards signal samples under a programmable threshold, is called *zero skipping* and can be considered a sort of L0 trigger.

Hits stored in the FIFO are 8b-10b coded, framed in “packets”, serialized, and transmitted at a maximum data rate fixed at 20 Mbps. The task of the FIFO is, thus, adapting the hit physical rate to the synchronous data rate of the transmitting channel. The overall data rate depends on many parameters: hit rate, hit duration, chosen threshold, number of pre-trigger samples, number of under-threshold samples, photocathode dimension, PMT high voltage. The expected hit rate with the NEMO 10” PMT was 50 kHz; allocating 100 bits per hit the expected data rate was 5 Mbps. Referring to real data analyzed from NEMO Phase1, about 130 bits per hit are needed, consisting of 16-bit threshold time, 10 samples and the packet overhead; the measured average hit rate is 80 kHz and the total data rate amounts to 10 Mbps, which is quite a bit higher than the expected 5 Mbps. Nonetheless the 20 Mbps available bandwidth can still accommodate the measured data rate.

Almost all of the slow control operations, such as parameters setting, sensors reading, high voltage PMT power supply control, FPGA programming, are accomplished by the DSP. An RS-232 serial port is also available and can be directly interfaced to an external peripheral.

Communication with the FCM is achieved by three twisted pair lines carrying the input clock signal, the low speed control channel, and the high speed output channel. Each line has a balanced differential interface terminated with a pair of transformers. Specifically, the clock line uses an LVDS receiver with very good performance in terms of jitter, while the two data lines use an RS-485 driver and an RS-485 receiver. The strength of the transmitted signal is limited by a passive circuit which can be adjusted according to the physical link length: this solution provides both a limitation of power consumption and lower interference with respect to the clock line.

The 5 MHz clock is fed to a Phased Locked Loop (PLL) device which multiplies the frequency up to 100 MHz. This clock drives both the FPGA, the ADCs, and the DSP. We chose to transmit the clock alone on a dedicated pair to minimize any possible jitter and noise over the link, because, at the very end, the timing resolution depends mainly on two factors: sampling clock jitter and quantization noise. After the PLL lock time we assume that all subsequent processes are synchronous with the received clock and their activation is deterministic. Moreover, the chosen PLL features a *Zero Delay* mechanism which aligns clock edges with a de-jittered version of the input clock, so that the FEM boards in the apparatus are synchronous and

<sup>2</sup>The power consumption of Fast ADCs does not scale linearly with the sampling frequency because different constructive technologies can be required to achieve higher performances. This was the case when the ADCs were firstly chosen in 2001.

<sup>3</sup>After pulses are PMT artifacts: if the programmable length of under threshold samples can merge after-pulses with a delay of few tens of nanoseconds with the true hit, the transmission packet with its overhead can be avoided and the data rate reduced.

phased<sup>4</sup>.

The second link pair carries an input bit stream, decoded by the FPGA, which has the same 5 Mbps rate of the line clock and contains slow control commands, such as acquisition parameters (threshold value, under-threshold tail length, ADCs offset, etc.), local sensors settings and commands, settings for PMT power supply. A special case is when commands need fixed execution latency: these commands are “intercepted” by the FPGA, parsed and executed without software intervention.

The third link pair provides the FEM board with an output channel of 20 Mbps maximum data rate. Both hits data and slow control information are merged by the FPGA and sent over this communication channel. If desired, some of the acquisition parameters (e.g. PMT high voltage monitor, temperature, humidity, average hit rate, pedestal values) can be either transmitted periodically or expressly requested for on-shore data logging.

Finally, board power is supplied using the common-modes of the two data line pairs and converted by high efficiency linear regulators to provide the needed supply voltages. The overall current consumption is 320 mA at 3.3 V.

#### IV. THE FLOOR CONTROL MODULE

The FCM can be thought of as a bridge between different communication protocols: on one side there is the optical fiber with a high speed serial link and a proprietary data format; on the other side there are many different devices each with specific physical and communication layers. In one direction the optical stream must be unpacked and demultiplexed to each destination device; in the other direction, the FCM collects many data streams from various sources, packs and outputs all the data onto the fiber acting as a multiplexer. Although the expected data rates for the two directions are different (much higher for underwater data) the link is fully symmetrical also thanks to the great amount of bandwidth available through the optical channel.

Fig. 4 is a picture of the FCM with the main interfaces and electronic components. The optical stream is fed to a mezzanine board, converted into the 800 Mbps electrical bit stream by the electro-optical *transceiver*, which, in turn, feeds the deserializer. On the other direction, data are encoded into a serial 800 Mbps stream by the serializer and then converted into optical signal.

The transceiver fulfills the Multi Source Agreement [17] standard which complies with ITU-T recommendations concerning Dense Wavelength Division Multiplexing (DWDM) data transmission. This technology allows multiplexing optical signals at different frequencies onto the same optical fiber, thus incrementing the communication channels without increasing the number of physical fibers. The transmission wavelengths can be chosen from a number of ITU prescribed values in a window around 1550 nm.

The receiver uses a Phased Locked Loop (PLL) to lock on the input data and extract the 40 MHz clock signal embedded in the serial bit stream. The extracted 16 bit words are then

available synchronously with the 40 MHz clock at the mezzanine interface. The NEMO communication protocol divides the stream in 125  $\mu$ s *frames* of 10000 bytes each, which are then distributed using a *positional* decoding mechanism: bytes in the payload are labeled by their position and each device is assigned a set of bytes in a specific but programmable range.

Both the programmable logic FPGA [18] in Fig. 4 and all the devices connected to the FCM are clocked by the locally re-synthesized and de-jittered clock provided by the receiver PLL, in order to maintain all the apparatus synchronous.

On the FCM *peripheral* side (see again Fig. 4), the FPGA exchanges floor information applying proprietary synchronous data interfaces with each device: optical modules, slow control (SCI), time calibration board (TCal), and a local digital signal processor (DSP). Each channel has its own electrical interface, communication protocol, and a dedicated FIFO memory inside the FPGA in order to adapt data rates to transmission rates over the optical channel. Collected data are then packed together using the same positional assignment mechanism explained above and transmitted through the optical link.

Regarding the OM electrical interface, all the arguments in section III hold but signal directions must be inverted. The FEM power supply is delivered by the FCM and is controlled by opto-switches, which connect two transformers center taps respectively to power and ground. A local ADC continuously monitors the current drawn by the optical module and, in case of abnormal consumption, automatically switch the power off to isolate any possible fault.

The DSP [19] runs many tasks: programming, monitoring and supervising both the electro-optical transceiver and the FPGA, being in charge of the local non-volatile memory used to store start-up codes, calibration tables, board parameters. The FCM is fully remotely re-programmable and both the FPGA and the DSP can be updated with new codes: a “safe” non-erasable code image is unconditionally loaded at power up to guarantee a working configuration with a proven communication with on-shore; new codes are stored in “extended” locations and can be loaded on demand.

The most important DSP task is providing the board with a PCI bus interface, needed on-shore to extract and insert data from/to the off-shore counterpart. The data rate supported by the PCI bus is 133 MB/s, which is largely enough for real-time data extraction: average data flow is expected to be less than 10 MB/s. This interface is also useful for board debugging, for easy and fast device reprogramming. Data are exchanged with the FCMI through DMA transfer using memory areas called Front End Buffers (FEB), as shown in Fig. 2. While slow control data are exchanged with the so-called *Data Manager*, physics data are sent to the first level trigger to be processed.

Referring to Fig. 1, each floor has its own Floor Power Module (FPM) which converts the high voltage of the electro-optical backbone providing three different voltages: +4.2 V, +5.5 V, and +12 V. The FCM, in turn, obtains the needed voltages regulating the +4.2 V, by means of low drop-out linear regulators, and switches the +5.5 V to FEM boards. The +12 V voltage is mainly used by oceanographic instruments.

Considering the design constraints presented in section I, the use of commercial devices, the high level of integration, and

<sup>4</sup>The clock path lengths between different FEM boards are supposed to be equal or, more realistically, known.

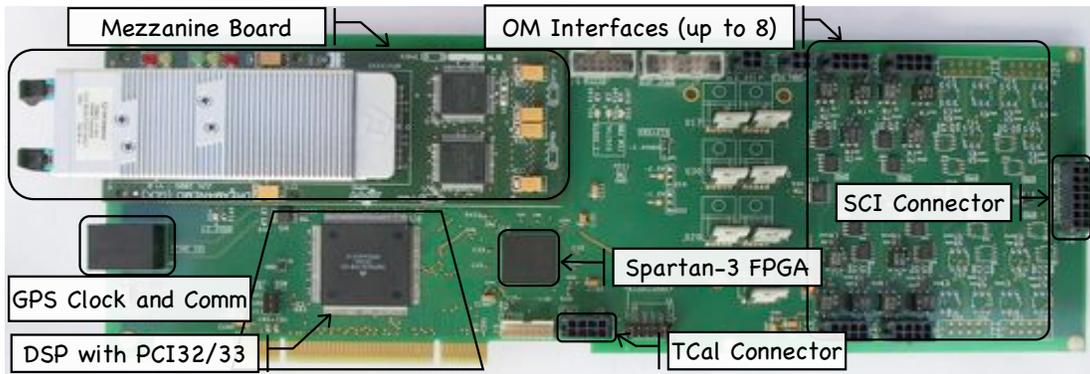


Fig. 4. Picture of the Floor Control Module with indication of relevant components.

the synchronous protocol, which needs only one communication interface, limit board dimensions to a full PCI-size card (about  $4'' \times 12.2''$ ). Power consumption amounts to 1.5 A at 3.3 V; the DWDM transceiver accounts for about 30% of the total power dissipated by the board.

The Slow Control Interface (SCI) board [20] was designed in a very flexible way to take care of floor slow peripherals. On the SCI board four micro-controllers, mapped on a Serial Peripheral Interface (SPI) [21] bus, let the environmental instruments and sensors communicate with the FCM. Information about seawater current velocity, salinity, temperature, data from the acoustical positioning system, as well as parameters referring to the internal state of the equipment, like humidity, temperature, power dissipation of attached peripheral, are collected altogether and sent to the FCM. Commands and data are received from the FCM on the SPI link to manage board parameters and control the instrumentation.

## V. THE TIME CALIBRATION

The synchronous protocol explained in section II was chosen both to simplify data transmission and to provide synchronization with a unique clock source.

A “timing station” is implemented on-shore for synchronization and calibration purposes: it distributes both a 4 MHz reference clock, derived from a GPS station, and a communication channel carrying information of GPS timing. On-shore FCMs are synchronized by this clock and can be time-aligned by a command code, issued every  $125 \mu\text{s}$ , to force the start of a frame; each frame can be identified with an identity code, which is the time counted in  $125 \mu\text{s}$  unit.

If the delay between the command and the start of a frame is constant, the on-shore transmitted data streams are synchronous and time-aligned. Each off-shore FCM, in turn, will receive a synchronous data stream misaligned only because of the different length of optical fibers which vary from floor to floor. While the optical paths vary, from an electronic point of view the delay equalization can be obtained using devices that exhibit a fixed latency in signal propagation. This requirement is more strict than the request of synchronicity, because it implies a fixed phase relationship between each link from on-shore to off-shore readout. Both the chip set on the FCM and the FEM guarantee by design this fixed latency property.

In order to allow the reconstruction of particle tracks, the front-end electronics must be able to tag “simultaneous” hits on different PMTs with the same time stamp. This constraint imposes that any difference in the elements belonging to the transmission chain must be compensated either with measurements or with procedures that allow a *self-calibration* or *equalization* of the system.

Even though the electronics ensures a fixed latency, the measurement of time offsets, due to different optical and electrical path lengths, must be performed: this is the goal of the time calibration procedure. The characterization of time offsets is divided in two parts: in the first one, the distance between the on- and off-shore FCMs is measured halving the time requested by a frame to go forth and back; this measurement gives a good approximation for absolute time alignment. The second part, applied only off-shore, consists of enlightening the optical modules of adjacent floors with the same light signal generated by a fast optical pulser and triggered by the FCM of one floor, so that a relative calibration from PMT to PMT and from floor to floor can be carried out<sup>5</sup>. The key point is that the trigger signal generated by the FCM

<sup>5</sup>The light signal is split and transmitted by means of optical fibers whose lengths have been characterized before the deployment.

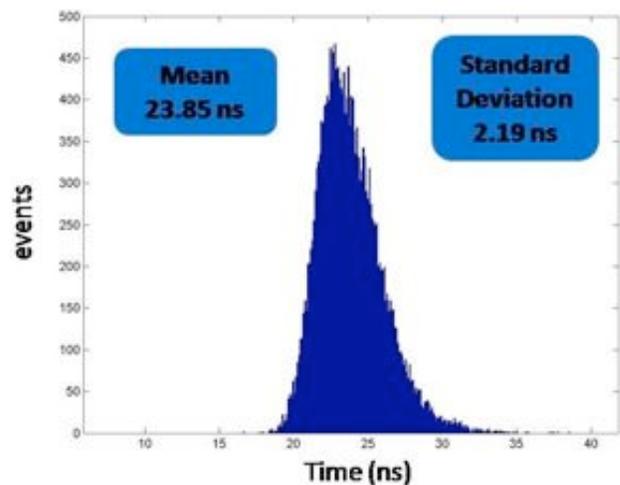


Fig. 5. Time acquisition values (modulo the pulser repetition period) of the signals induced by the time calibration pulser on OM0 of the second floor.

is always emitted with a fixed delay with respect to the frame start, which in turn has a fixed delay with respect to the GPS time: since all the elements of this chain have fixed latency, differences in time stamping can be attributed only to different link paths. Hence this measurement allows a relative and very precise alignment of time stamps.

The mentioned procedure relies on the so-called Time Calibration (TCAL) board [22]: this board can be controlled from on-shore through allocated bytes in the payload: data exchange with the FCM uses a simple electrical interface to switch the board on and off, to set the pulser optical power, and to emit the trigger signal which activates calibration pulses at a 8 kHz repetition rate.

As an illustration of the timing calibration procedure, we show in Fig. 5 the histogram of the time stamps related to hits generated by the time calibration pulser. Time stamps are calculated modulo  $125 \mu\text{s}$ . In the figure, the signals induced by the pulser accumulate in a peak which can be well fitted with a Gaussian curve. The mean value of this curve gives the necessary information for estimating the time offset of the PMT, while the standard deviation gives a measurement of the overall stability of the system, typically of the order of 2.2 ns. This result is also useful to set an estimate of the time resolution capabilities of the readout. In fact, the main contribution to this value comes from the PMT Transit Time Spread which has a standard deviation of about 2 ns. The remaining contribution is due to the LED pulser, the fibers and the splitting system, the clock transmission, and the front-end electronics. Thus the time resolution of the readout is, as requested, sub-nanosecond. More details on the results of the timing calibration procedure may be found in [23].

## VI. RESULTS

In this section some results obtained with the currently working apparatus and aimed to qualify the acquisition electronics will be described. Next figures show graphs calculated analyzing *raw* data acquired on the 17<sup>th</sup> of February, 2007, from the first OM on the third floor.

Fig. 6 displays the charge histogram calculated on  $8 \times 10^5$  raw hits. Waveforms have been decompressed to invert the

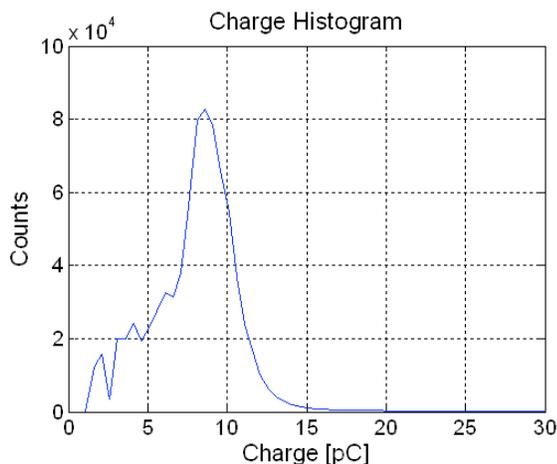


Fig. 6. Charge histogram of raw hits for OM0 on third floor.

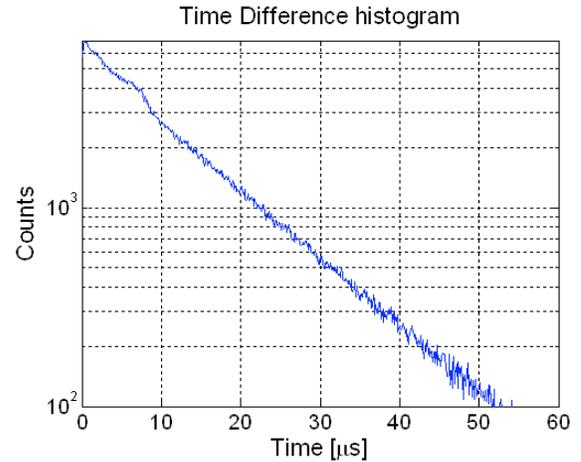


Fig. 7. Hit time stamp differences histogram of raw hits for OM0 on third floor.

non-linear effect of analog compression, converted into current values, and integrated to produce the charge. The clearly visible peak is centered around the expected 8 pC *spe* value, as the PMT gain has been set to  $5 \times 10^7$ . The rough behavior at small charge values is due to the high acquisition threshold and to the 1 pC binning. Each PMT on all floors behaves much like the others, showing a very good uniformity in the gain values and an extremely distinct peak for the *spe* charge.

Using the same set of data, in Fig. 7 the histogram of time differences between consecutive hits is shown: since the hits due to the background take place according to a Poisson probability distribution, the separation in time of consecutive hits follows an exponential distribution as verified by the semi-log chart which shows a straight line. The mean data rate corresponding to this distribution is about 82 kHz.

The small yet apparent excess below  $8 \mu\text{s}$ , indicating a strong correlation outside of the exponential distribution, is due to PMT after-pulses: the number of hits is about 8% which corresponds to what stated in Hamamatsu data sheet for the R7081-SEL photo-multiplier in use.

The FEM measures the average hit rate in a 10 ms interval and sends the result to the Data Manager. The time development of the average rate values of the fourth OM in the fourth floor is shown in Fig. 8: data were collected during 18 hours starting from the 10<sup>th</sup> of January 2007. The thick plateau at about 73 kHz is the hit rate baseline, due to the

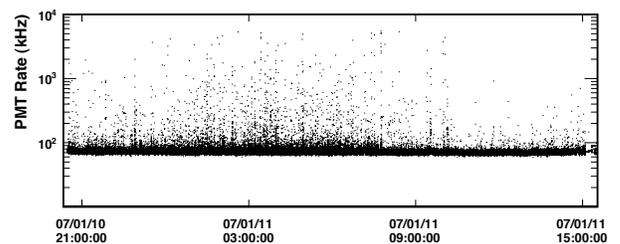


Fig. 8. Average hit rate, calculated once per second on a 10 ms interval, versus time for OM4 on fourth floor.

contribution of both  $^{40}\text{K}$  and diffused bioluminescence; the high peaks emerging from the baseline and reaching values up to 5 MHz are caused by localized bioluminescence activity.

Fig. 9 shows the histogram of average rate values displayed in Fig. 8; some significant parameters can be calculated from the histogram: fitting the peak with a Gaussian distribution yields a Gaussian mean of 71.9 kHz, while the median is 73.5 kHz, and the average rate is 81.3 kHz.

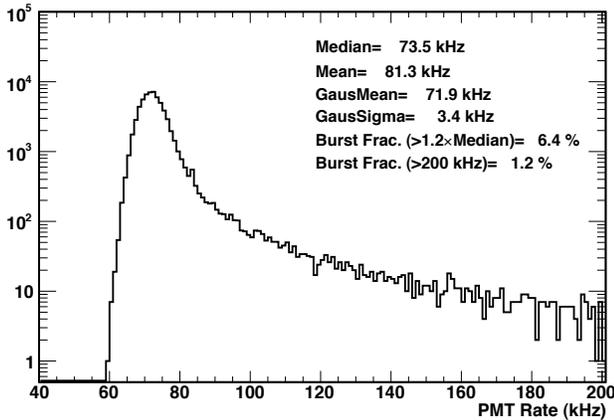


Fig. 9. Histogram of hit rate values shown in Fig. 8.

All the graphs shown in this section refer to specific PMTs: actually corresponding figures could be presented for the other PMTs of the deployed mini tower but they are all very similar and do not add any further information.

## VII. CONCLUSIONS

The strategy applied to the design of the data acquisition and transmission system for the NEMO experiment, successfully tested in the NEMO-Phase1 prototype deployed in December 2006 at the NEMO Test-Site, has been described in this paper. The NEMO-Phase1 operation has shown that the PMT digitizing electronics, the FEM board, all the floor electronics, and the FCM board, fulfill all of the project requirements: especially, the low power consumption per channel, which amounts to less than 4 W (taking into account also the instrumentation), and the simple optical link architecture, which requires just one wavelength per floor and one fiber per tower, meet the main requirements.

The link between on- and off-shore uses optical fibers because of the considerable distance of the underwater apparatus from the coast: DWDM, chosen to reduce the number of required fibers, appears to be a reliable and mature technology available off-the-shelf, though electronic components are still rapidly changing.

The FCM board, thanks to its symmetry, is also used on-shore plugged into a PCI bus to allow communication with the off-shore board. The choice of using the same board, even though not optimized, permitted a faster development, simpler design and production, and an easier debugging phase.

The safe reprogrammability feature has been shown to be extremely important not only to correct possible problems but also to tune the system after data analysis: during NEMO Phase1 the FEM acquisition code has been changed in the

field to deal with the observed bioluminescence level and to optimize data taking.

One advantage of using a PC to host the FCM is the large amount of memory and computing power available: in fact instead of sending all raw data to first level triggers some local screening could be already implemented, thus simplifying data distribution and decreasing the network load. One drawback of this scheme is that, even though up to 3 FCMs could share the same PCI bus, this could become a problem when more floors are added; currently a new FCM board, compatible with the old one, is under design and will be provided with an on board *Gigabit Ethernet* interface, so that there will be no more need to plug it into a PC.

Data available on-shore through the Front End Buffers, located in the hosting PC memory, have been extensively analyzed to check the validity of both the acquisition modules and the transmission system. Various results have been illustrated in section VI, showing very good performance of the system. The agreement of the graphs with expected results indicate also that both the acquisition itself and the post-processing (e.g. the signal decompression) are implemented correctly and satisfy the required constraints.

All of this information contributes heavily to the design of future electronics which can be further tailored to suit the needs of successive stages of analysis.

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