RPC Trigger Overview

presented by Maciek Kudla, Warsaw University

RPC Trigger ESR
Warsaw, July 8th, 2003
RPC Trigger Task

The task of RPC Muon Trigger electronics is to deliver 4 highest momentum muons in the barrel and 4 highest momentum muons in endcaps to the Global Muon Trigger (GMT).

PACT decision is elaborated from the RPCs signals (NIM A434 (1999) 90-95, NIM A456 (2000) 143-149) and from those of H0 calorimeter scintillators (CMS Note 2003/draft 17.03.2003).

To fulfill this task and guarantee the trigger quality all trigger data are delivered to the CMS DAQ. Local, selective readout and diagnostic tools are used to test whole chain of the trigger system.
General layout

Detector

Front End Boards (FEBs)

Link Boxes (LBxs)

Hcal H0

distance max 16 m

electrical cables ~10 k (11,5)

Detector Periphery

distance 90 m

RPC Trigger Racks

to GMT
2* 4 muons

to DAQ
3 Slinks

Counting Room

Front End Boards (FEBs) on RPCs - F.Loddo

Link Boxes (LBx) on detector - K. Pozniak

Trigger Crates in USC55 - my talk this afternoon

(*) - with RE5
Front end electronics task

- Discrimination of the RPC strip signals (threshold to be set up)
- Fix length pulse generation (pulse duration to be set up)
- Data transmission to the Link system
- Control of the FEB is made from Link system via I2C interface. FEBs inputs can be tested by the test pulses sent from Link system

Front End Electronics = Front End Board (FEB)
Link system task

Receiving of the FEB data, synchronization to LHC clock
Data transmission to the Trigger system (USC 55)
FEB control
Diagnostics (test pulses to the FEBs, histograms, selective readout)
Control of the Link system is made via CCU base DCS system (and via TTC distribution system)

Link system = Link Boxes (Link Boards (Master or Slave) + Control Boards)

1 Master Link Board - 1 opto link
FEB - LBx interface

LBx:

6 * FEB data cables
6 * FEB I2C cables
   FEB data cable - 40 pin Scotchflex connector
   FEB I2C cable - 10 pin Scotchflex connector

LBx/RE11:

8 * FEB data cables
8 * FEB data cables
   FEB data cable - 40 pin Hpack 2mm connector
   FEB I2C cable - 40 pin Hpack 2mm connector
   (1 connector - 4 channels)

details - K. Pozniak presentation
Trigger electronics task

Receiving of the LBxs data

Data synchronisation and transmission to the PAttern Comparator (PAC) processors

Muon search (PAC processors) and muon sorting tree

Diagnostics (selective readout)

Trigger electronics = Trigger Racks (Trigger Crates (Trigger Boards + ...))

12 Trigger Crates + 1 Sorter Crate in 8 Racks
Data links from Detector to Trigger Crates (1)

Very low data rate (CMS Note 2000/068) of the RPC chambers allows for the compression scheme (NIM A 419 (1998) 701-706), which reduces the number of the optical links by the factor of 6.

The principle of the compression scheme used in PACT link system is to send only the non-zero fragments of the RPC data in consecutive periods of the 40 MHz LHC clock.

Data from several RPCs can be send by one data link, The content of the data links are defined is such a way that
1. data loss will not exceed 1%,
2. the number of links needed on the Trigger boards will be bigger than 20.

For details see CMS IN 2002/065.
Data links from Detector to Trigger Crates (2)
<table>
<thead>
<tr>
<th></th>
<th>without RE5</th>
<th></th>
<th>with RE5</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>sector</td>
<td>total</td>
<td>sector</td>
<td>total</td>
</tr>
<tr>
<td>opt. links</td>
<td>55</td>
<td>660</td>
<td>63</td>
<td>756</td>
</tr>
<tr>
<td>TB opt. Inputs</td>
<td>136</td>
<td>1632</td>
<td>146</td>
<td>1752</td>
</tr>
</tbody>
</table>
Trigger data optical link

Link 1600 Mbps has been selected

Serializer - GOL chip (32 bits/LHC clock)
Transmitter - Vcsel Honeywell HFE 4191-541
fiber - multimode
Opto receiver (on TB) - Stratos dual receiver M2R- 25-9-1- TL
Deserializer - Tlk 2501

details - K.Pozniak presentation
Task of the splitters is to split one optical signal into 2 or 4 destinations. On the total 660 RPC trigger opto links (without RE5):
- 70 goes to unique location on TB,
- 396 goes to 2 locations on TB,
- 192 goes to 4 locations on TB.
In addition H0 needs 108 1=>2 splitters.

**Prefered solution**

- PIN Diode
- LC Connectorized
- VCSEL
- LC Connectorized
- 1.6Gbps
- Fan out
Input parameters:

* consider RE1/1 station (worst case), 1/2 chamber/lmux
* 1 crate: 48 links
* streamer probability: 1%
* strip multiplicity w/out streamers: 1.1 strips
* strip multiplicity with streamers: 6.5 strips

<table>
<thead>
<tr>
<th>number of packets/event</th>
<th>no noise</th>
<th>100Hz/cm² noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>average/link</td>
<td>0.04</td>
<td>0.065</td>
</tr>
<tr>
<td>average/crate</td>
<td>3.14</td>
<td>4.59</td>
</tr>
<tr>
<td>max/crate (10⁶ events)</td>
<td>14</td>
<td>17</td>
</tr>
</tbody>
</table>

To the DAQ zero compressed data from the input of the TB are send (the same form as on LB). Average event size will not exceed several hundreds kB

3 Slink to DAQ are proposed, still big safety factor
RPC Trigger Rack

Trigger electronics I will present this afternoon - here only very short introduction:

Trigger Rack (6)

Trigger Crate (12)

Trigger Board (9)

Sorter Crate (1)

Sorter Board (4)

Readout Conc. Board (3)

RPC Trigger ESR, Warsaw, July 8, 2003

Ignacy Maciek Kudla, Warsaw University
Prototypes - Link Board 1 (Altera) -1

- first version of LB
- Synch and Lmux - Altera Acex 100
- GOL mezzanine board
- TTCrx board
- 96 LVDS FEB signals, old connector
- only VME interface, FPGA download from VME only
Prototypes - Link Board 1 (Altera) -2

- optical transmission test setup - receiver board
- optical transmission test setup - SFF transmitter
- optical transmission test setup - VCSEL
- 2001 synch tests
- transmission tests - 10^{-12} achieved in lab tests with both optical transmitters

Mohsine (Marseille) Board: Infineon Tlk 2501 APEX
Prototypes - Link Box RE11 - Link Board

- Link Board for RE11
- Synchro FPGA
- Lmux (data coder) FPGA
- Link Board Controller FPGA (here Acex has to be replaced by Actel)
- Flash memory (on the other side of the board) ……..
- GOL and Vcsel
- VME interface (optional here)
- used CERN tests 2003
- Control Board for RE11
- TTCrx distribution
- CCU
- Control Board Controller (Altera Acex here must be partially replaced by Actel)
- VME interface (optional here only, for tests)
- used CERN Synch tests 2003
Prototypes - Link Box RE11- Back plane

- Back plane for the RE11 Link box
- control bus
- CSC connectors
- FEB I2C connectors
- FEB data connectors
- CCU connectors
- TTC opto connector
- trigger data opto connector
- used CERN tests 2003

Link Box RE11- LB, CB Boards without back plane
Prototypes - Receiver Board

- opto receiver VME board (+ several mezzanine boards) for
  * optical link tests
  * synchro FPGA tests
  * Ldemux tests and PAC tests
  * DAQ derandomizer and Slink tests
- PC mezzanine for testing without VME
- status - Rec Board in tests, Slink interface board in production, Pac board in design
Prototypes - Readout Boards

Set of readout boards - master and slave - first RPC FED prototype (1999)
- readout slave channel FPGA - Flex 8k
- derandomizer memory - external
- TTCrx board
- FED buffer
- event builder
- VME interface, FPGA download from VME only
- used CERN tests 1999

now all buffer memories inside of FPGA's!
Prototypes - Trigger Board

Trigger board 1999, many mezzanine boards
- Synchro, Readout (derandomizer) FPGA (here pipeline inside FPGA)
- PAC (still ASIC, but also FPGA)
- PC (with Ethernet)
- Sorter, Control (Jtag Controller), Readout concentrator FPGAs
After change to wedge architecture only one partition for RPC muon is possible.

<table>
<thead>
<tr>
<th>TTCvi</th>
<th>1</th>
</tr>
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<tbody>
<tr>
<td>TTCex</td>
<td>2</td>
</tr>
<tr>
<td>TTCoc/16</td>
<td></td>
</tr>
<tr>
<td>UXC barrel</td>
<td></td>
</tr>
<tr>
<td>wheel</td>
<td>=&gt; 2</td>
</tr>
<tr>
<td>total</td>
<td>=&gt; 10</td>
</tr>
<tr>
<td>UXC endcap</td>
<td></td>
</tr>
<tr>
<td>RE1,2+RE1/1</td>
<td>=&gt; 2 * 2</td>
</tr>
<tr>
<td>RE3</td>
<td>=&gt; 2 * 1</td>
</tr>
<tr>
<td>RE4</td>
<td>=&gt; 2 * 1</td>
</tr>
<tr>
<td>total</td>
<td>=&gt; 8</td>
</tr>
<tr>
<td>USC</td>
<td></td>
</tr>
<tr>
<td>total</td>
<td>=&gt; 1</td>
</tr>
<tr>
<td>total</td>
<td>=&gt; 19</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>TTCrx</th>
</tr>
</thead>
<tbody>
<tr>
<td>UXC (equal to # of (LB + CB))</td>
</tr>
<tr>
<td>total</td>
</tr>
<tr>
<td>USC (equal to # of crates)</td>
</tr>
<tr>
<td>total</td>
</tr>
<tr>
<td>total</td>
</tr>
</tbody>
</table>
RPC muon trigger deliver to GMT 4 highest momentum muons from barrel and 4 highest momentum muons from endcap.

Information send to GMT (one muon = one cable) are following:
- phi address - 8 bits
- eta address - 6 bits
- pt - 5 bits
- quality - 3 bits
- sign, valid sign - 2 bits
- control (clock, BCN0, bcn(2..0), SEr) - 6 bits
(address form still under discussion)

Parallel LVDS has been selected for data transfer.
SCSI- 3 connectors, type of LVDS drivers, pin assignment were agreed.
Cable selection under discussion

Data are send to GMT from USC55 RPC Trigger Rack D7

see CMS Note IN 2003/000 for details
# Inventory

<table>
<thead>
<tr>
<th>Trigger Crate</th>
<th>12</th>
</tr>
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<tbody>
<tr>
<td>Trigger Board</td>
<td>108</td>
</tr>
<tr>
<td>Timing&amp;Readout Board</td>
<td>12</td>
</tr>
<tr>
<td>Trigger Crate back plane</td>
<td>12</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Sorter Crate</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sorter Board</td>
<td>4</td>
</tr>
<tr>
<td>Timing&amp;Readout Board</td>
<td>1</td>
</tr>
<tr>
<td>Readout Concentrator Board</td>
<td>3</td>
</tr>
<tr>
<td>Sorter Crate back plane</td>
<td>1</td>
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<table>
<thead>
<tr>
<th></th>
<th>without RE5</th>
<th>with RE5</th>
</tr>
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<tbody>
<tr>
<td><strong>Link Box</strong></td>
<td>108</td>
<td>132</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Link Board</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master Link Board</td>
<td>588</td>
<td>684</td>
</tr>
<tr>
<td>Slave Link Board</td>
<td>980</td>
<td>1124</td>
</tr>
<tr>
<td>Control Board</td>
<td>228</td>
<td>276</td>
</tr>
</tbody>
</table>

| **Link Box RE11**    | 12          | 12      |
|                      |             |         |
| **Link Board RE11**  |             |         |
| Master Link Board    | 72          | 72      |
| Control Board        | 12          | 12      |

| **Fiber Link**       | 660         | 756     |